

MS-G019

Ver: 2.1

mini-ITX : 192 * 180 mm

SOC:

Intel - Braswell M/D

OnBoard Chipset:

AUDIO:REALTEK/ALC662-VD0

LAN:REALTEK/RTL8111G-CG

SIO:NUVOTON/NCT6793D

Flash ROM: 64Mb SPI (SOC)

Main Memory:

DDRIII L SO-DIMM(1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot*1

Mini-PCIE connector*1

PWM:

VCCP:ON Semiconductor/NCP81201MNTXG

VGG:ON Semiconductor/NCP81201MNTXG

VNN:TI/TPS51211DSCR

DDR:TI/TPS51216RUKR

Other:

SATA2.0 x2

USB2.0 RearX4 Front X2

USB3.0 RearX4

DP to D-SUB*1/HDMI*1

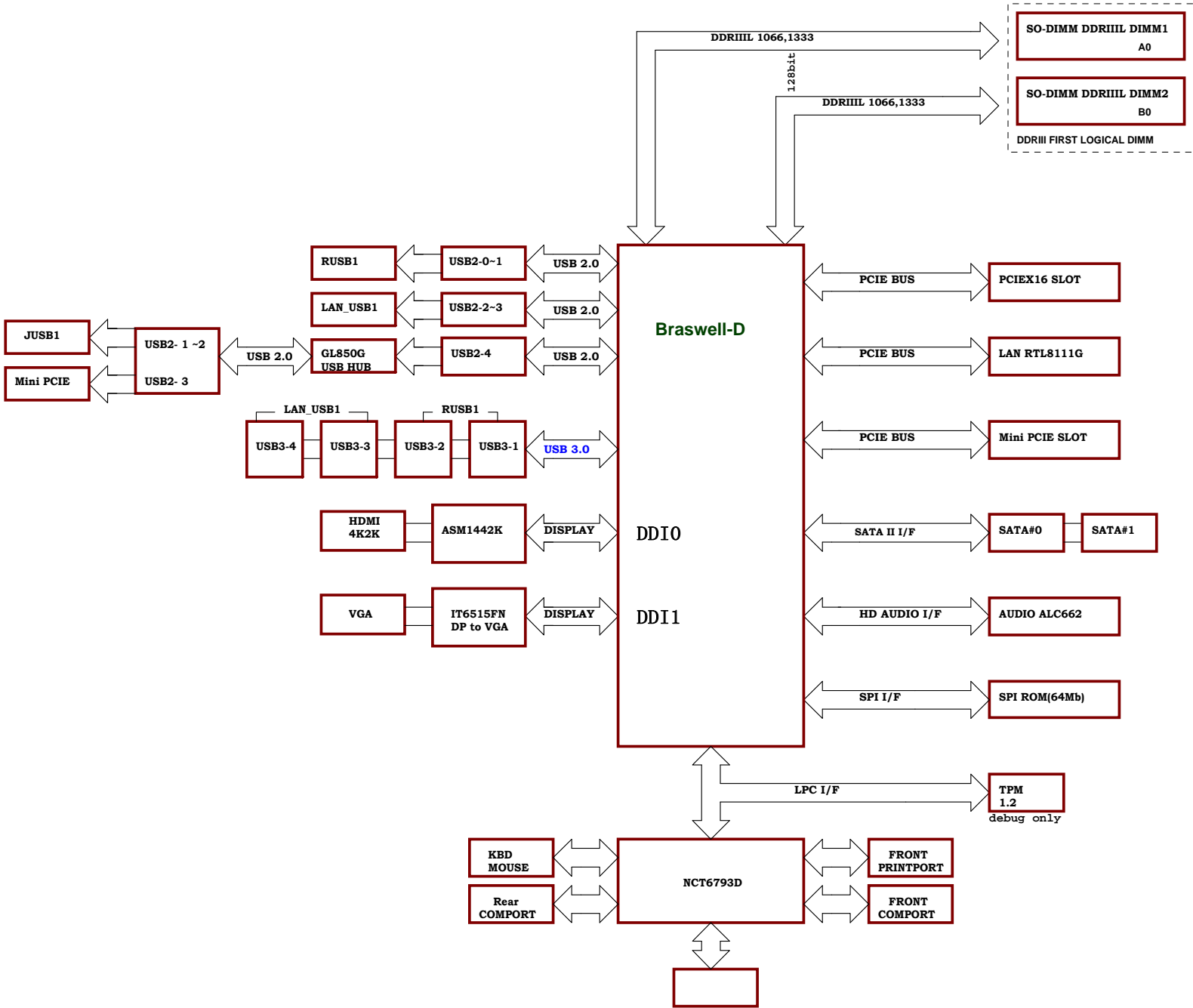
LPT Header *1

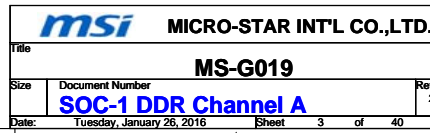
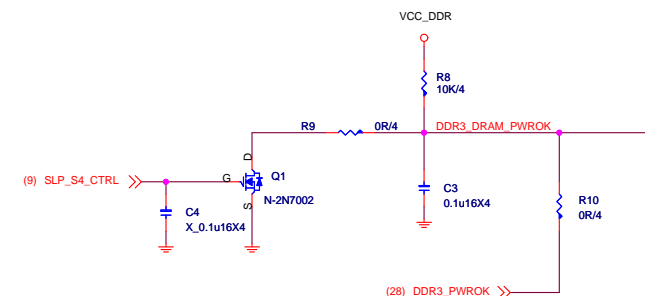
Rear COMPORT *1

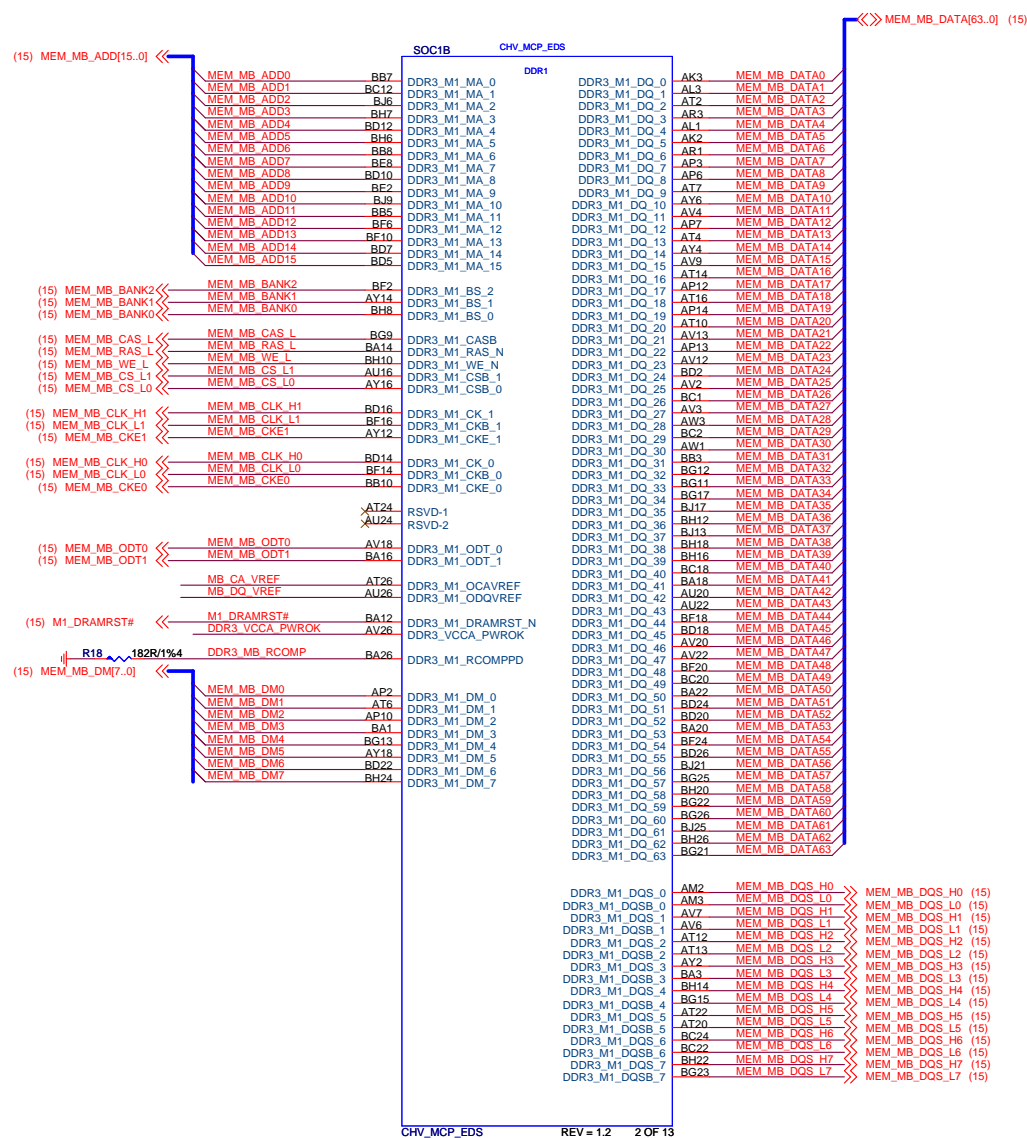
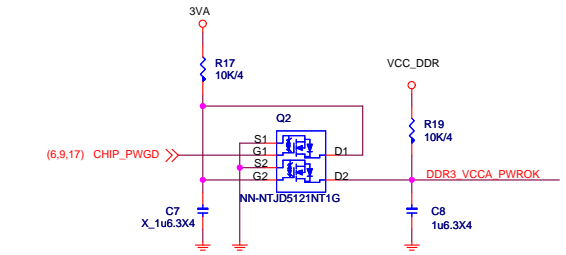
Front COMPORT *1

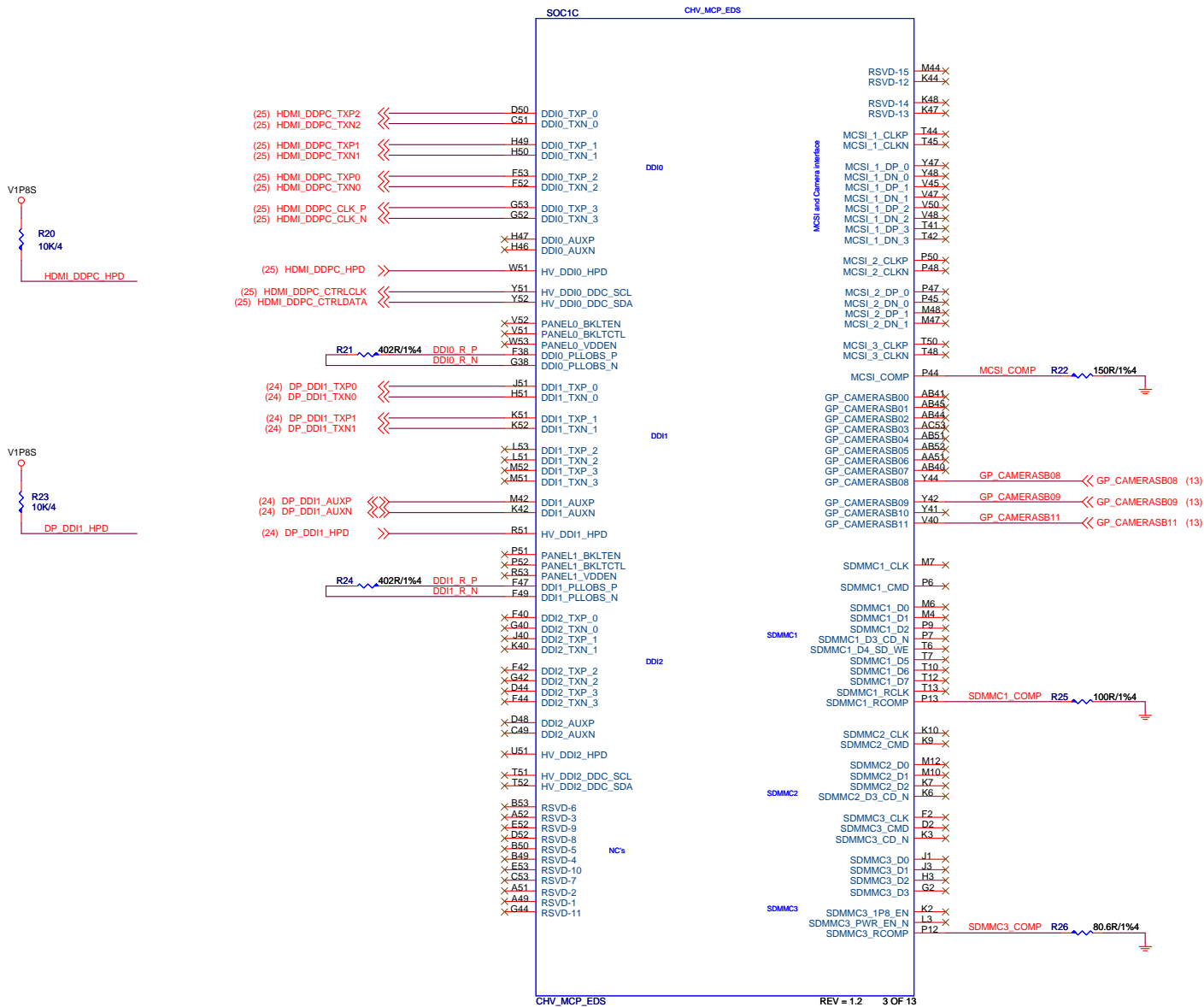
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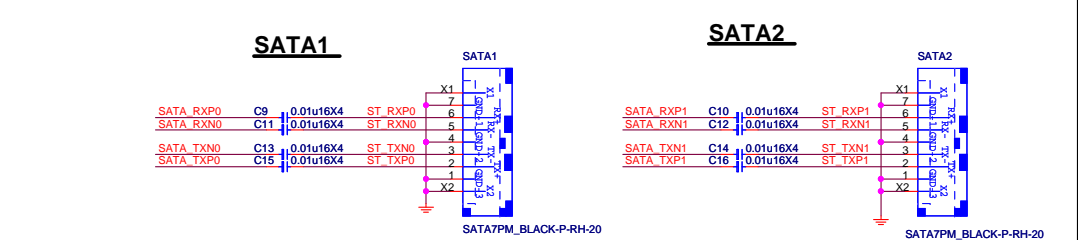
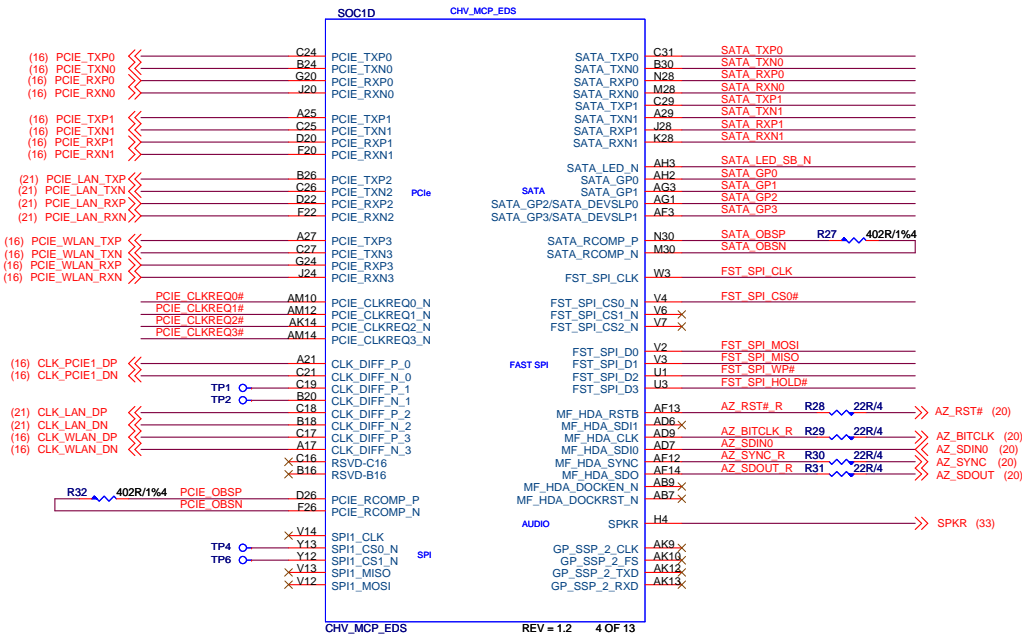
Model type	Function Options	BOM Config	ERP BOM No.	BOM Opt.
		CFG-G019-030	601-G019-	
		CFG-G019-040	601-G019-	A





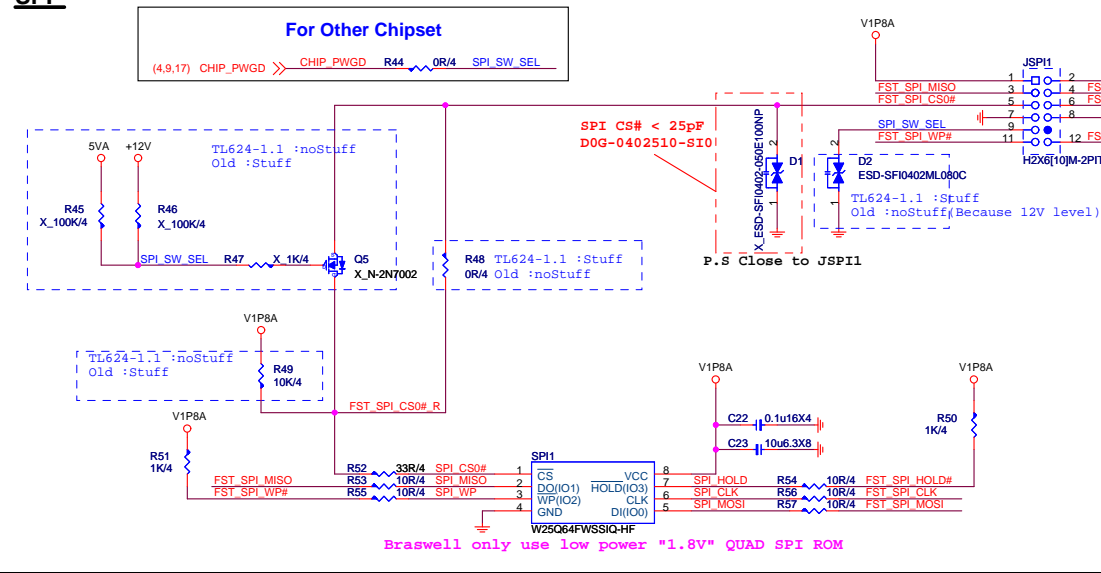


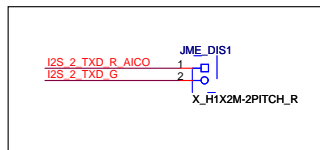
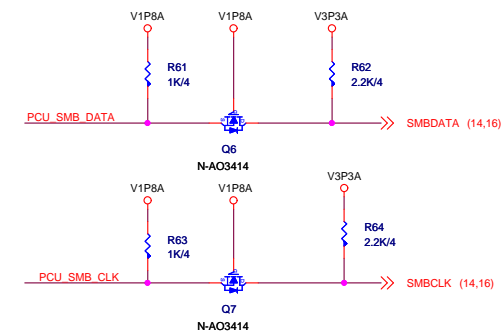
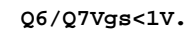


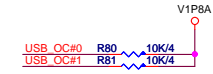
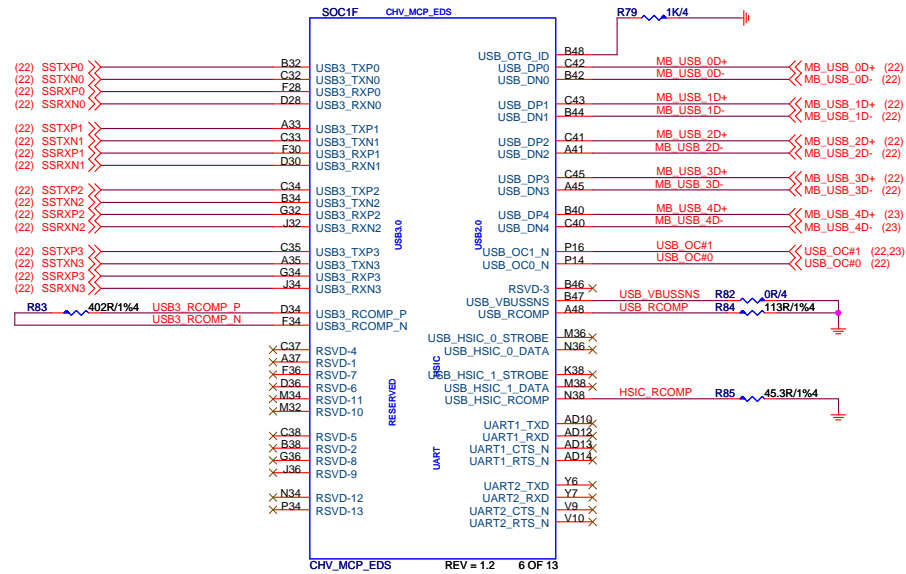


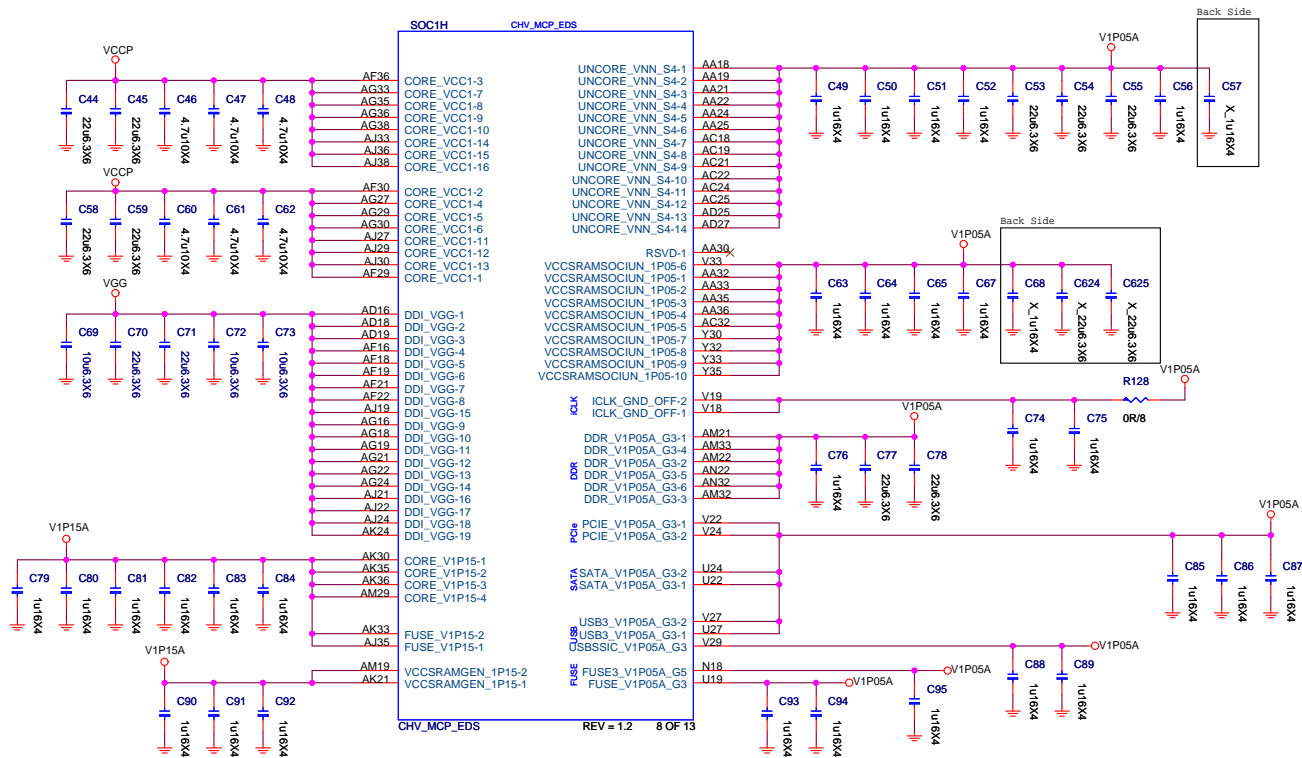
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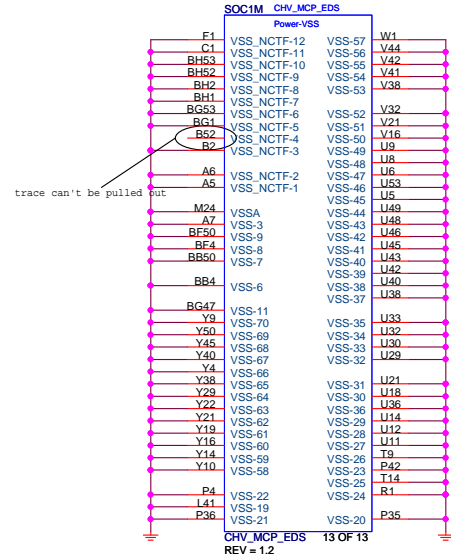
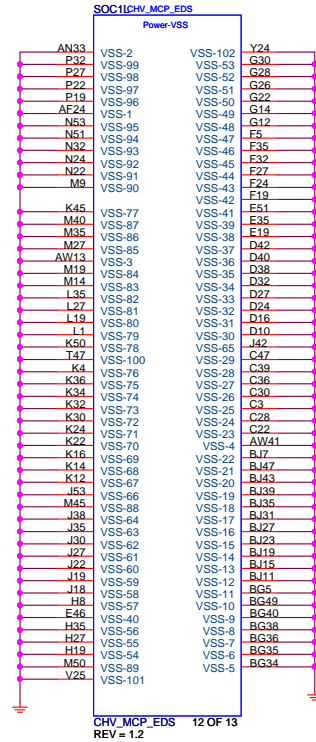
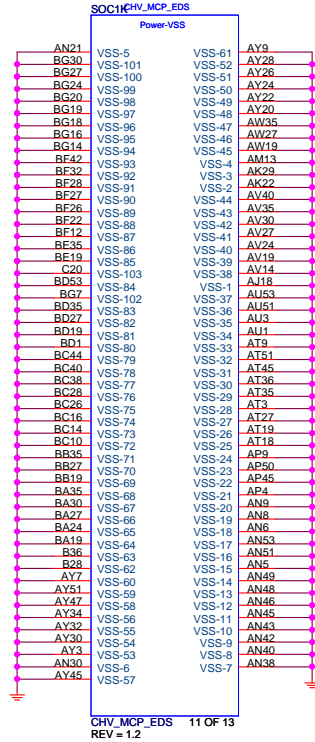
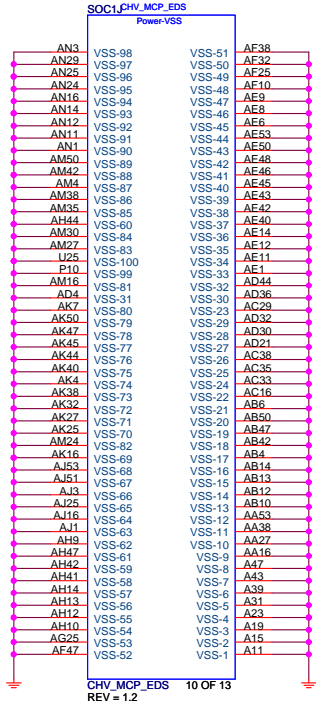
SPI











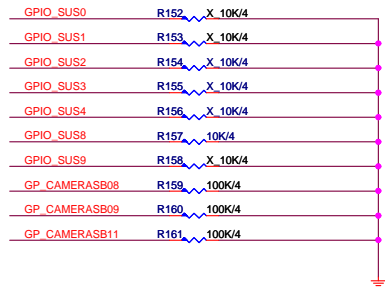
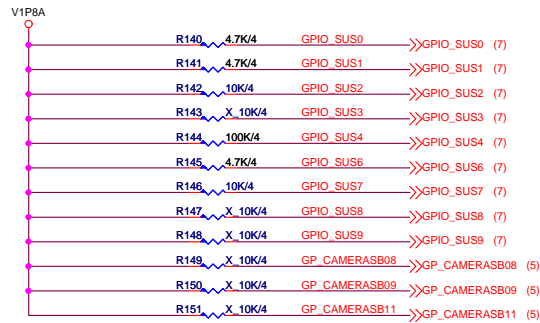


Table 24-1. Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port	How to Disable Port
DDI0	GPIO_SUS0	Pull-up to V1P8A with 4.7-K Ω \pm 5% resistor	N/A, Weak internal pull-down
DDI1	GPIO_SUS1	Pull-up to V1P8A with 4.7-K Ω \pm 5% resistor	N/A, Weak internal pull-down

Note: DDI2 is always enabled an no Hard Strap is needed.

Table 2-26. Hard Strap Description and Functionality (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal (20k PD)	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal (20k PD)	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	Top Swap (A16) override	Weak internal (20k PU)	0 = Change Boot Loader address 1 = Normal Operation
GPIO_SUS[3]	MIPI-DSI Display Detect	Weak internal (20k PD)	0 = DSI Port not detected 1 = DSI Port detected Note: DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the pin floating if GPIO functionality is not used.
GPIO_SUS[4]	Boot BIOS Strap (BBS)	Weak internal (20k PU)	0 = No SPI (Default) 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal (20k PU)	0 = Not supported 1 = Normal Operation
GPIO_SUS[6]	Halt Boot Strap	Weak internal (20k PU)	1 = Normal Operation Note: This strap MUST be High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	Weak internal (20k PU)	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal (20k PD)	0 = No bypass 1 = Bypass with 1.05V

Table 2-26. Hard Strap Description and Functionality (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	Weak internal (20k PD)	0 = No Bypass (Default) 1 = Bypass

SODIMM #A0 (STD) N13-2040930-CK3 9.2H

(3) MEM_MA_ADD[15..0]

MEM_MA_ADD0 98
MEM_MA_ADD1 97
MEM_MA_ADD2 96
MEM_MA_ADD3 95
MEM_MA_ADD4 92
MEM_MA_ADD5 91
MEM_MA_ADD6 90
MEM_MA_ADD7 89
MEM_MA_ADD8 86
MEM_MA_ADD9 85
MEM_MA_ADD10 107
MEM_MA_ADD11 84
MEM_MA_ADD12 83
MEM_MA_ADD13 119
MEM_MA_ADD14 80
MEM_MA_ADD15 78

(3) MEM_MA_BANK0
(3) MEM_MA_BANK1
(3) MEM_MA_BANK2
(3) MEM_MA_CS_L0
(3) MEM_MA_CS_L1
(3) MEM_MA_CLK_H0
(3) MEM_MA_CLK_L0
(3) MEM_MA_CLK_H1
(3) MEM_MA_CLK_L1
(3) MEM_MA_CKE0
(3) MEM_MA_CKE1
(3) MEM_MA_CAS_L
(3) MEM_MA_RAS_L
(3) MEM_MA_WE_L

R165 10K/4 SA0 DIM0_0
R166 10K/4 SA1 DIM0_0
SMBCLK_DDR
(15) SMBDATA_DDR

(3) MEM_MA_ODT0
(3) MEM_MA_ODT1
(3) MEM_MA_DM[7..0]

MEM_MA_DM0 11
MEM_MA_DM1 28
MEM_MA_DM2 46
MEM_MA_DM3 63
MEM_MA_DM4 136
MEM_MA_DM5 153
MEM_MA_DM6 170
MEM_MA_DM7 187

(3) MEM_MA_DQS_H0
(3) MEM_MA_DQS_H1
(3) MEM_MA_DQS_H2
(3) MEM_MA_DQS_H3
(3) MEM_MA_DQS_H4
(3) MEM_MA_DQS_H5
(3) MEM_MA_DQS_H6
(3) MEM_MA_DQS_H7
(3) MEM_MA_DQS_L0
(3) MEM_MA_DQS_L1
(3) MEM_MA_DQS_L2
(3) MEM_MA_DQS_L3
(3) MEM_MA_DQS_L4
(3) MEM_MA_DQS_L5
(3) MEM_MA_DQS_L6
(3) MEM_MA_DQS_L7

MEM_MA_DQS_H0 12
MEM_MA_DQS_H1 29
MEM_MA_DQS_H2 47
MEM_MA_DQS_H3 64
MEM_MA_DQS_H4 137
MEM_MA_DQS_H5 154
MEM_MA_DQS_H6 171
MEM_MA_DQS_H7 188
MEM_MA_DQS_L0 10
MEM_MA_DQS_L1 27
MEM_MA_DQS_L2 45
MEM_MA_DQS_L3 62
MEM_MA_DQS_L4 135
MEM_MA_DQS_L5 152
MEM_MA_DQS_L6 169
MEM_MA_DQS_L7 186

DIMM1A

A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC#
A13
A14
A15

BA0
BA1
BA2
S0#
S1#
CK0
CK0#
CK1
CK1#
CKE0
CKE1
CAS#
RAS#
WE#
SA0
SA1
SCL
SDA

ODT0
ODT1

DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7

DQS0
DQS1
DQS2
DQS3
DQS4
DQS5
DQS6
DQS7
DQS#0
DQS#1
DQS#2
DQS#3
DQS#4
DQS#5
DQS#6
DQS#7

DDR3SODIMM-204PS_BLACK-HF-35

SMBCLK_DDR R170 33R/4 <<>>SMBCLK (7,16)
SMBDATA_DDR R171 33R/4 <<>>SMBDATA (7,16)

<<>> MEM_MA_DATA[63..0] (3)

MEM_MA_DATA5
MEM_MA_DATA1
MEM_MA_DATA7
MEM_MA_DATA3
MEM_MA_DATA0
MEM_MA_DATA4
MEM_MA_DATA6
MEM_MA_DATA2
MEM_MA_DATA10
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MEM_MA_DATA62

VCC_DDR

75 VDD
76 VDD
81 VDD
82 VDD
87 VDD
88 VDD
93 VDD
94 VDD
99 VDD
100 VDD
105 VDD
106 VDD
111 VDD
112 VDD
117 VDD
118 VDD
123 VDD
124 VDD

VCC3

77 NC1
122 NC2
125 NCTEST
198 EVENT#
30 RESET#

VREF_DQ_A

VREF_CA_A

VREF_DQ

VREF_CA

VSS

VSS

VSS

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DIMM1B

44 VSS
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66 VSS
71 VSS
72 VSS
127 VSS
128 VSS
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138 VSS
139 VSS
144 VSS
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150 VSS
151 VSS
155 VSS
161 VSS
162 VSS
167 VSS
168 VSS
172 VSS
173 VSS
178 VSS
179 VSS
184 VSS
185 VSS
189 VSS
190 VSS
195 VSS
196 VSS

VDDSPD

77 NC1
122 NC2
125 NCTEST
198 EVENT#
30 RESET#

VREF_DQ

VREF_CA

VSS

VSS

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Pin 205/Pin 206 PAD

VCC_DDR

EC1
C100016S0
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C153

C154

C162

C155

C156

C157

C158

C159

C160

C161

C163

C164

C165

C166

C167

C168

C169

C170

C171

C172

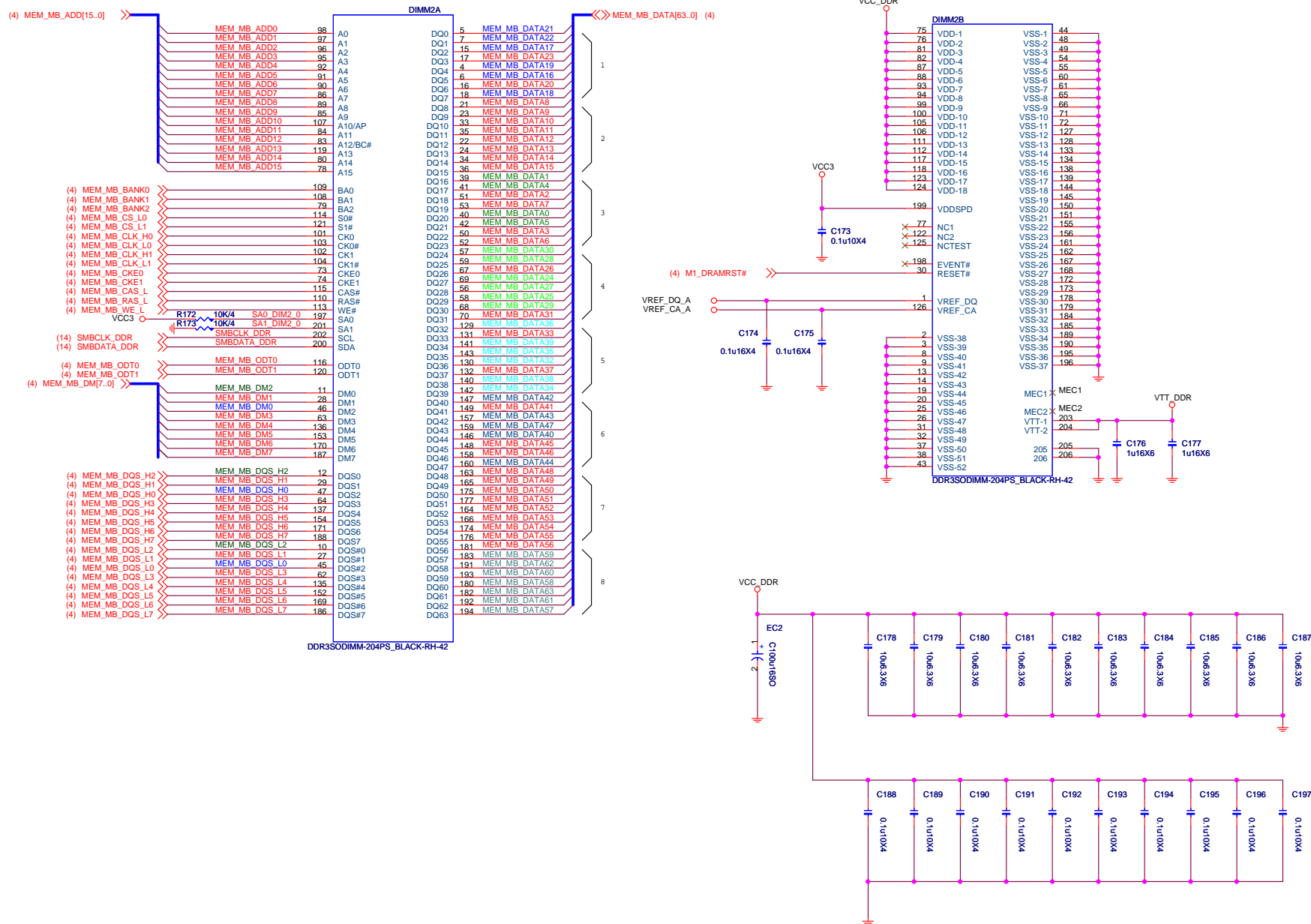


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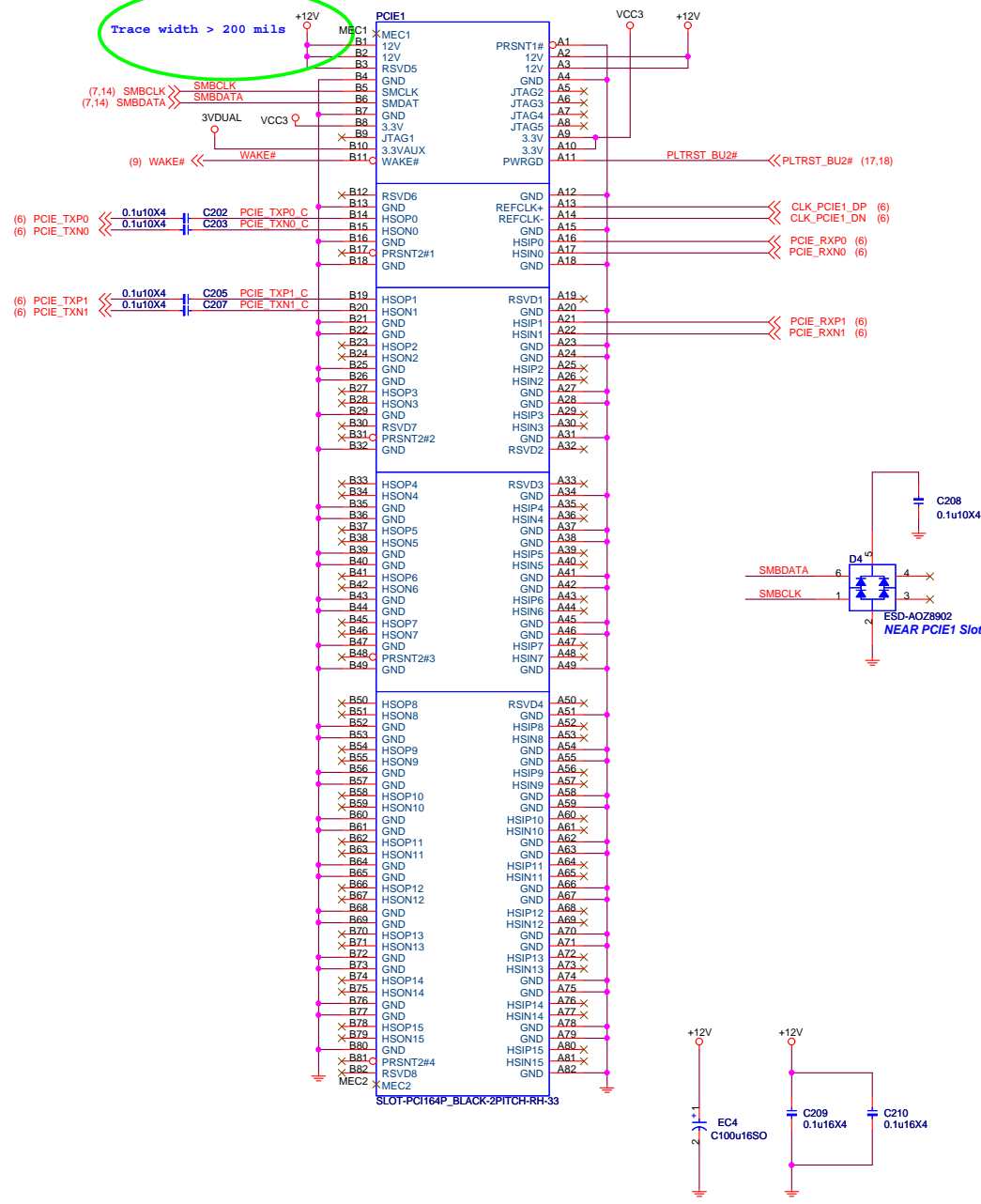
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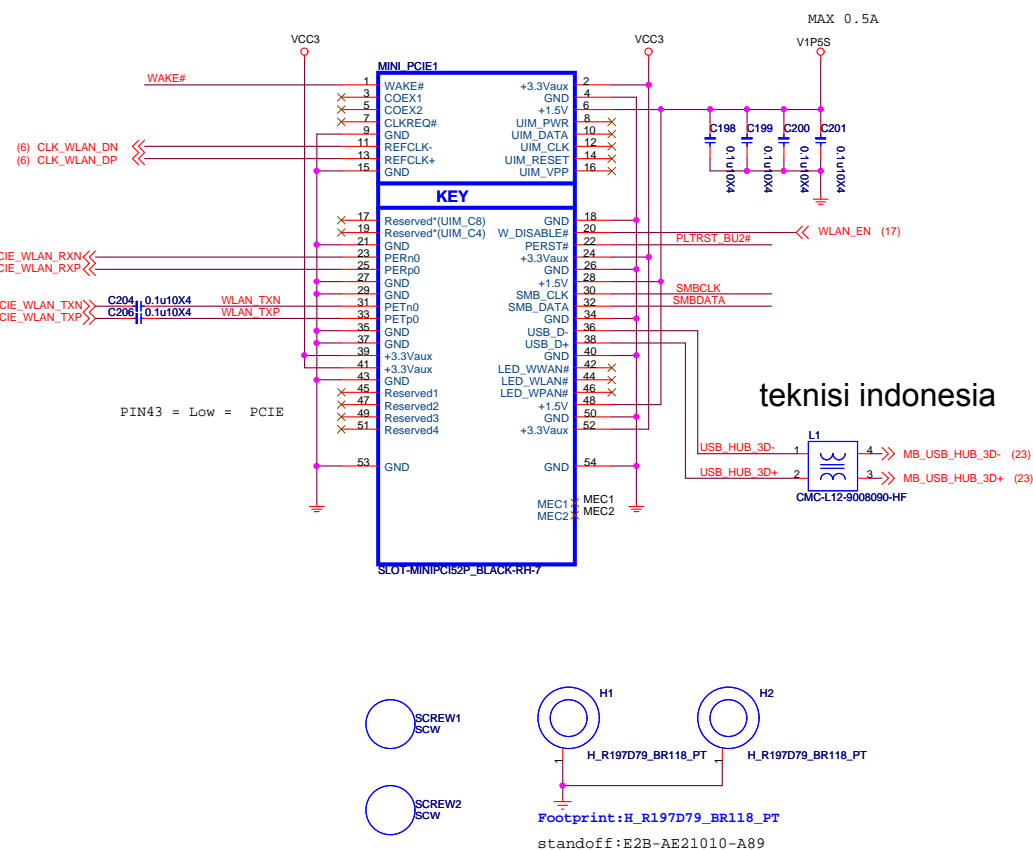
N13-2041200-CK3 9.2H



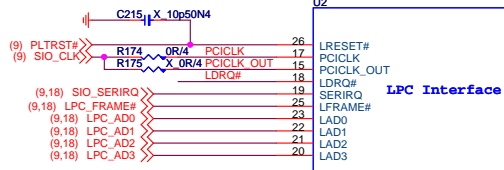
PCI Express X16 Slot



Mini-PCIEX1



Footprint:H_R197D79_BR118_PT
standoff:E2B-AE21010-A89



Printer mode

SLCT/CIRRXWB0/GP46

ACK#/GP43/DGL_0#

ERR#/GP36/DGL_1#

AFD#/GP35/DGH_1#

SOUTB_P80/STB#/GP34

INIT#/GP41/SCL/MSC

GP2/2/SUS/ATX/OUT4#

PD0/KB_SCN1/GP60/LED_A

PD1/KB_SCN2/GP61/LED_B

PD2/KB_SCN3/GP62/LED_C

PD3/KB_SCN4/GP63/LED_D

PD4/KB_SCN5/GP64/LED_E

PD5/KB_SCN6/GP65/LED_F

PD6/GP66/LED_G

PD7/GP67/DGH_0#

GRN_LED

YLW_LED

RIA#/GP87

DCDA#/GP86

(P80_EN)SOUTA_P80/SOUTA/GP85

SINA/GP84

(TEST_MODE0_EN)DTRA#/GP83

(2E_4E_SEL)RTSA#/GP82

DSRA#/GP81

CTSA#/GP80

RIB#/GP10

DCDB#/GP11

(TEST1MODE_EN)IRTX0/SOUTB/GP12

IRRX0/SINB/GP13

(UARTB_P80_EN)DTRB#/GP14

(UARTA_P80_EN)RTSB#/GP15

DSRB#/GP16

CTSB#/GP17

(DDR4_EN)GA20M

KBRST#

GP23/MCLK

GP22/MDAT

GP21/KCLK

GP20/KDAT

LATCH_BKFD_CUT#/GP33/3VBSW#

NC

PCHVSB

VTT

VBAT

CASEOPEN#

3VA-1

3VA-2

3VCC-1

LPC_VDD

AVSB

VREF

VSS-1

VSS-2

CPUD-/AGND

CP1 X_COPPER

CP2 X_COPPER

CP3 X_COPPER

CP4 X_COPPER

CP5 X_COPPER

CP6 X_COPPER

CP7 X_COPPER

CP8 X_COPPER

CP9 X_COPPER

CP10 X_COPPER

CP11 X_COPPER

CP12 X_COPPER

CP13 X_COPPER

CP14 X_COPPER

CP15 X_COPPER

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CP232 X_COPPER

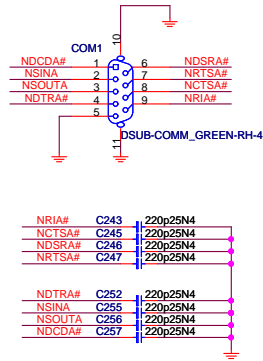
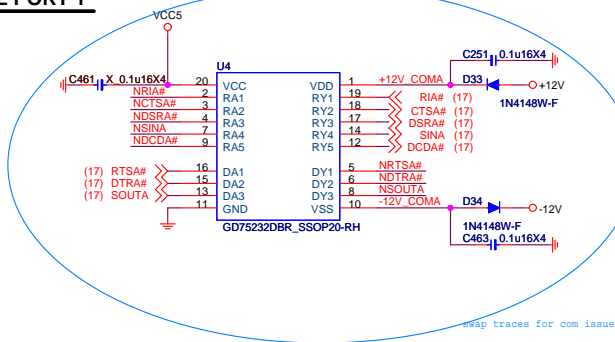
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CP234 X_COPPER

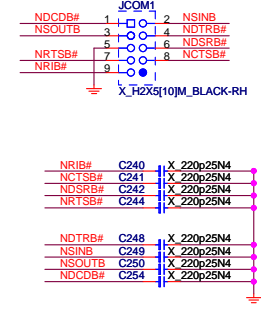
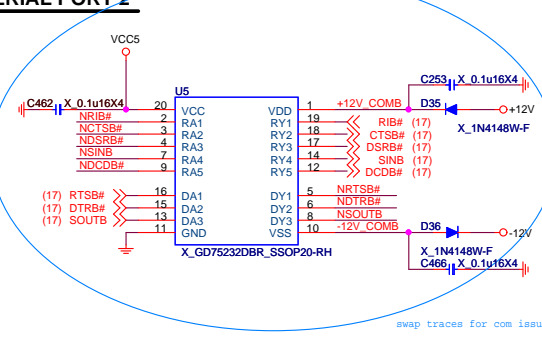
CP235 X_COPPER

CP236 X_COPPER

SERIAL PORT 1

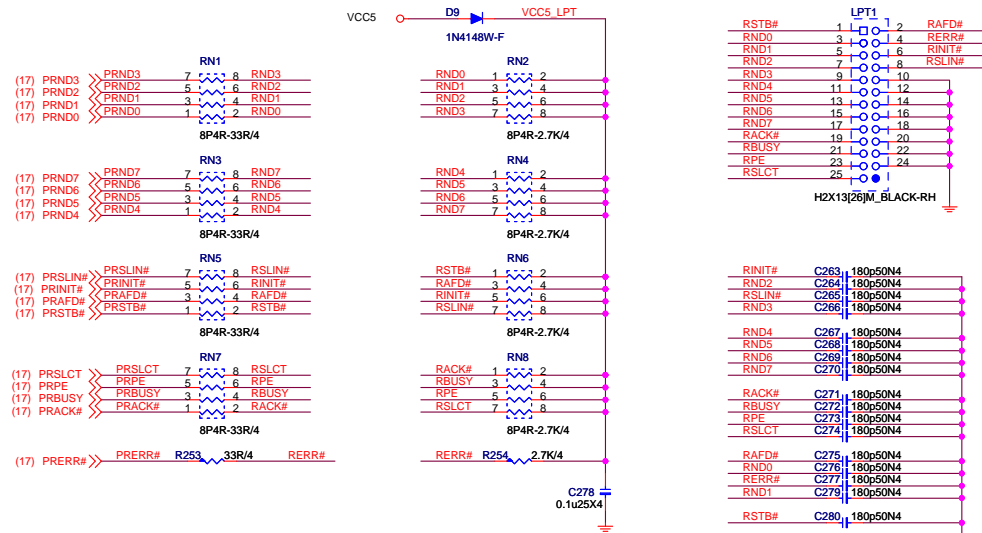


SERIAL PORT 2

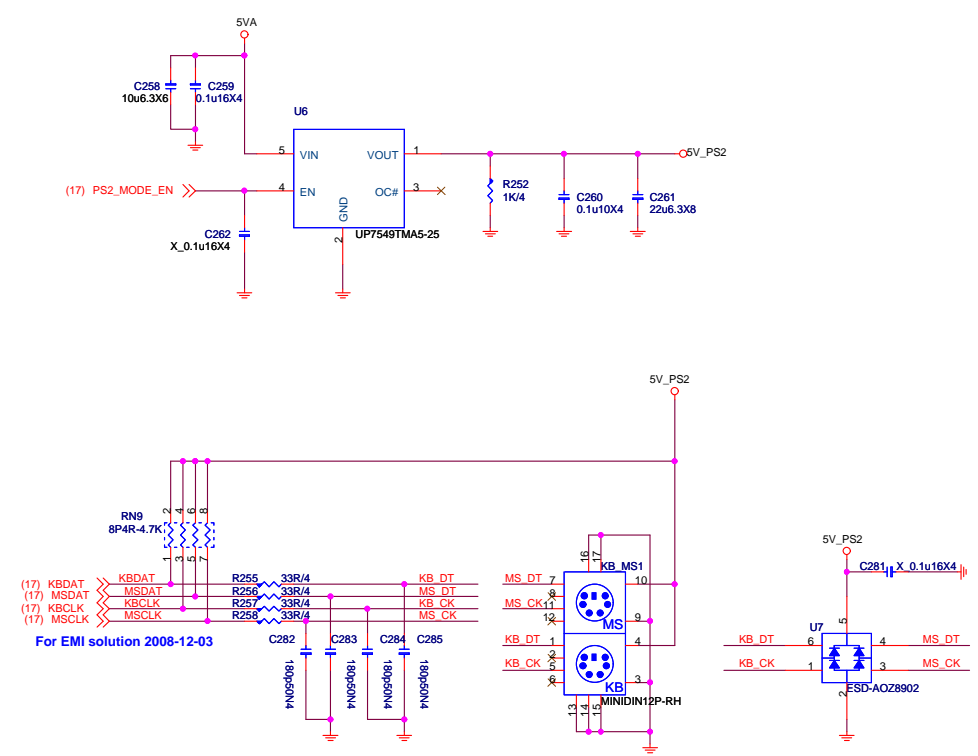


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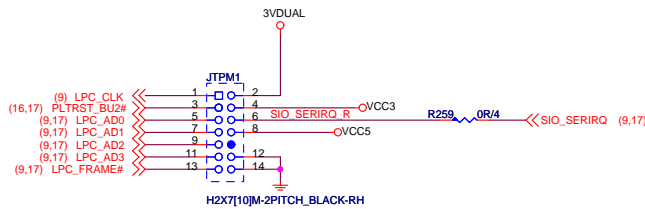
PARALLAL PORT



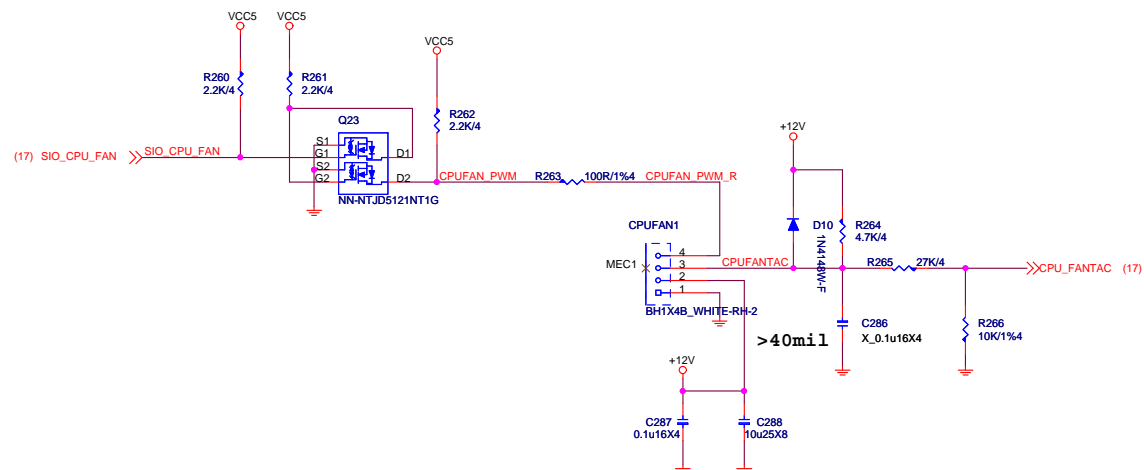
PS2 KEYBOARD & MOUSE CONNECTOR



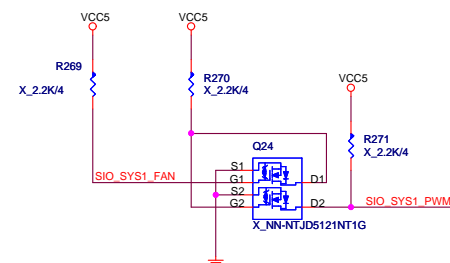
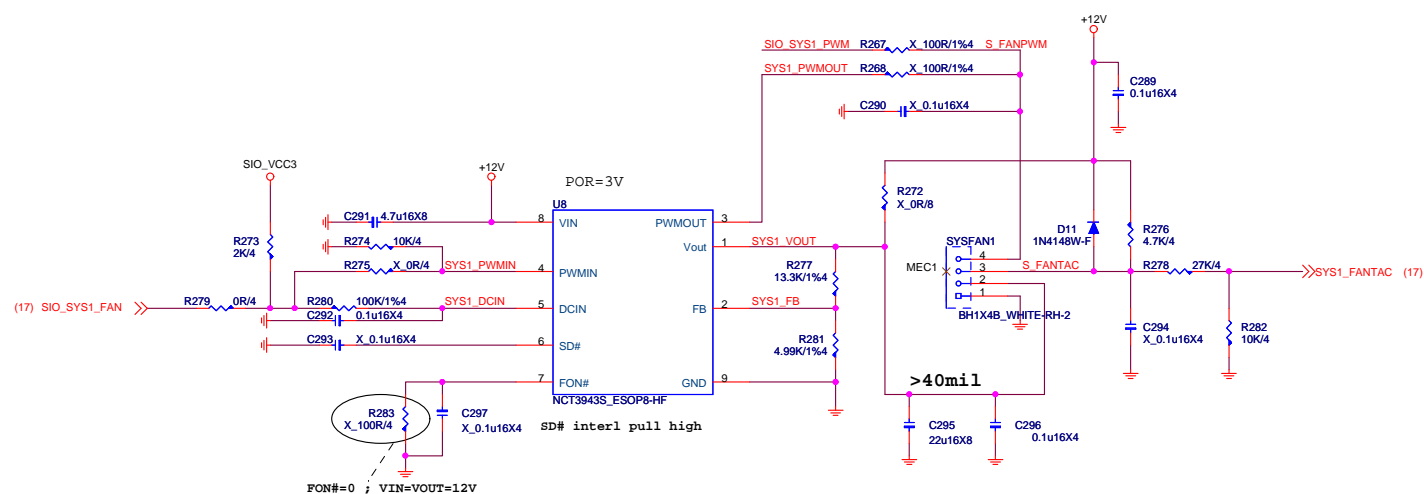
TPM/JLPC



CPUFAN

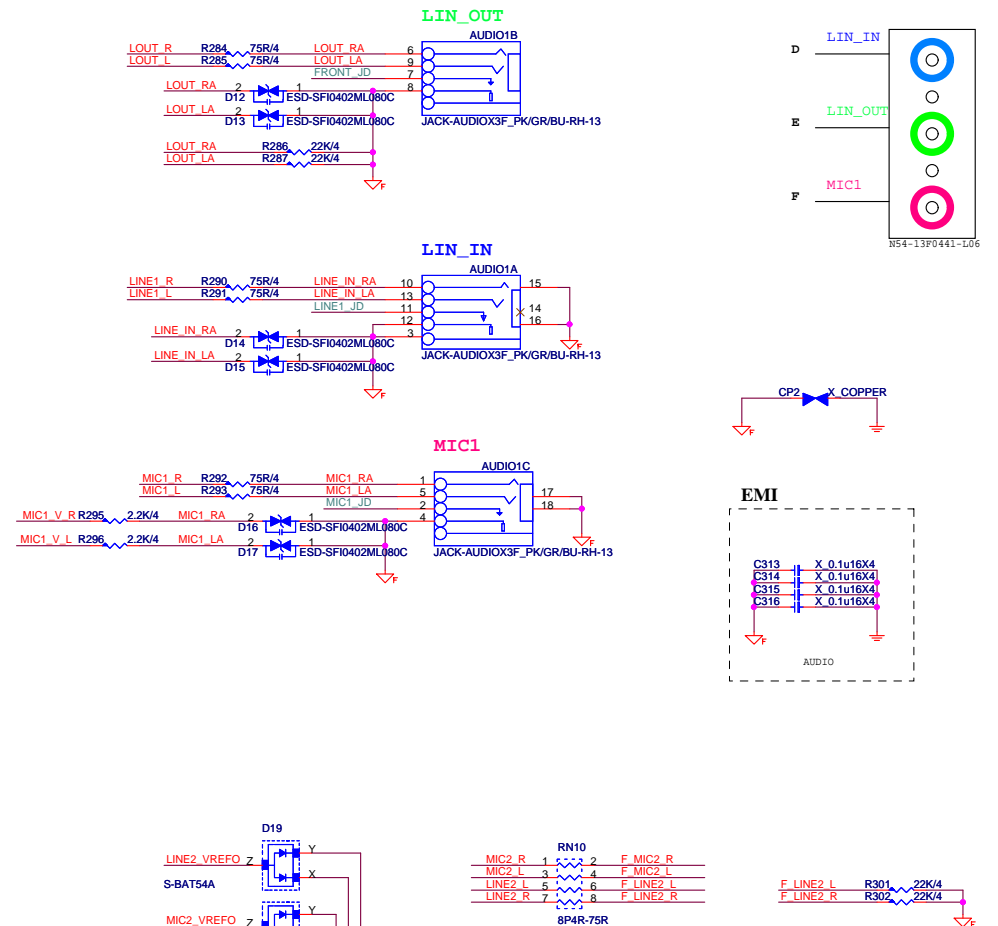
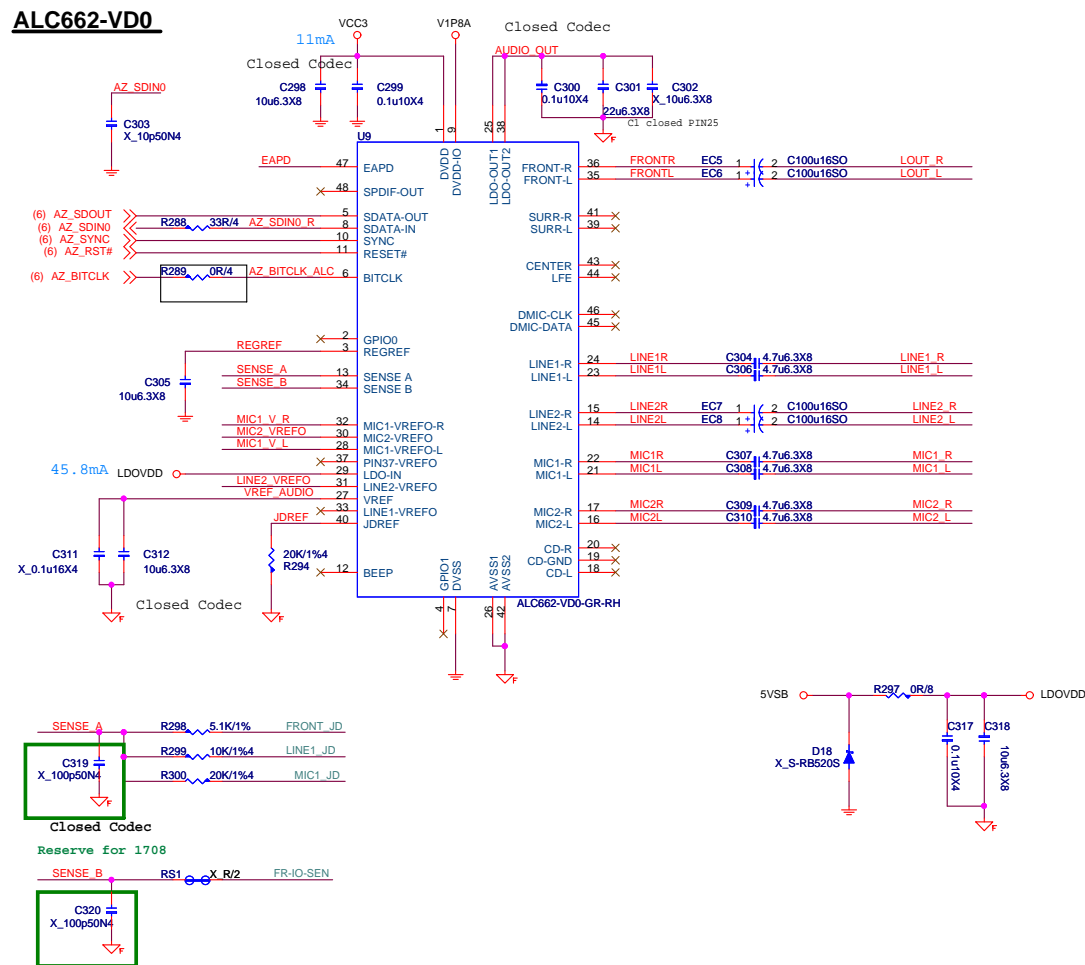


SYSFAN



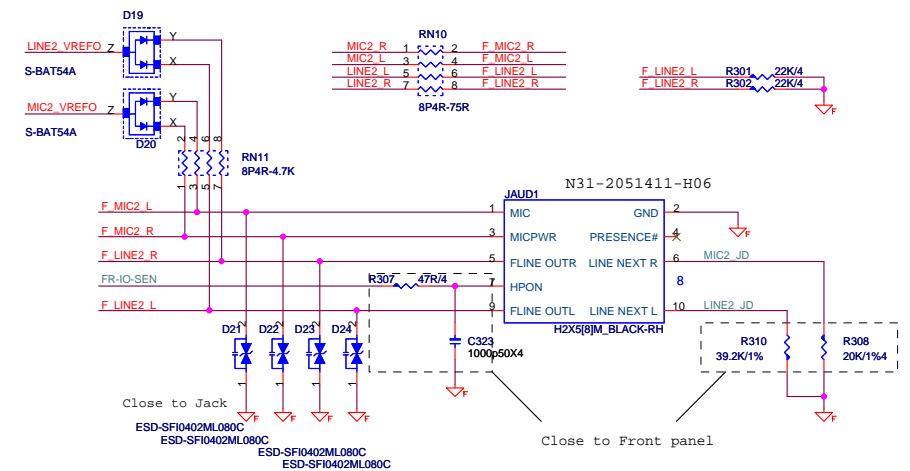
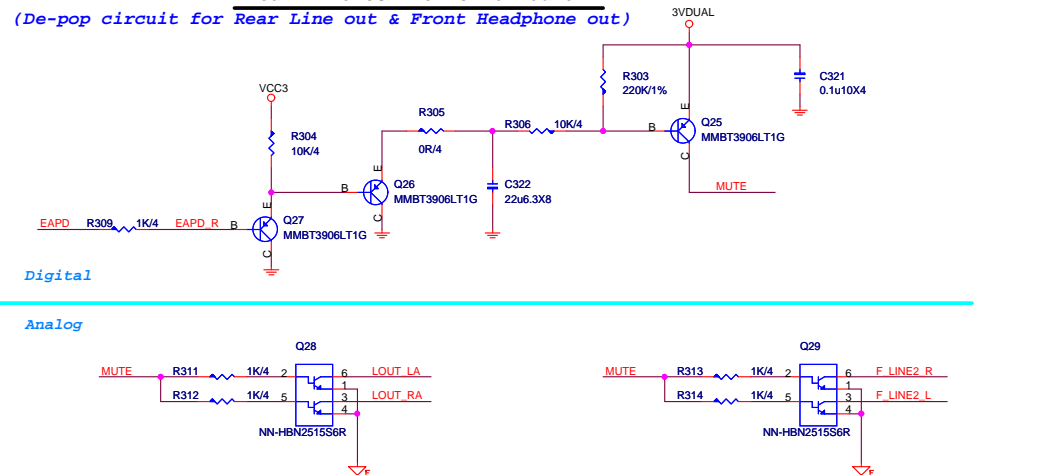
SYSFAN_PWR_OFF
SIO control
Close SIO_SYS1_FAN Vout=0

ALC662-VD0

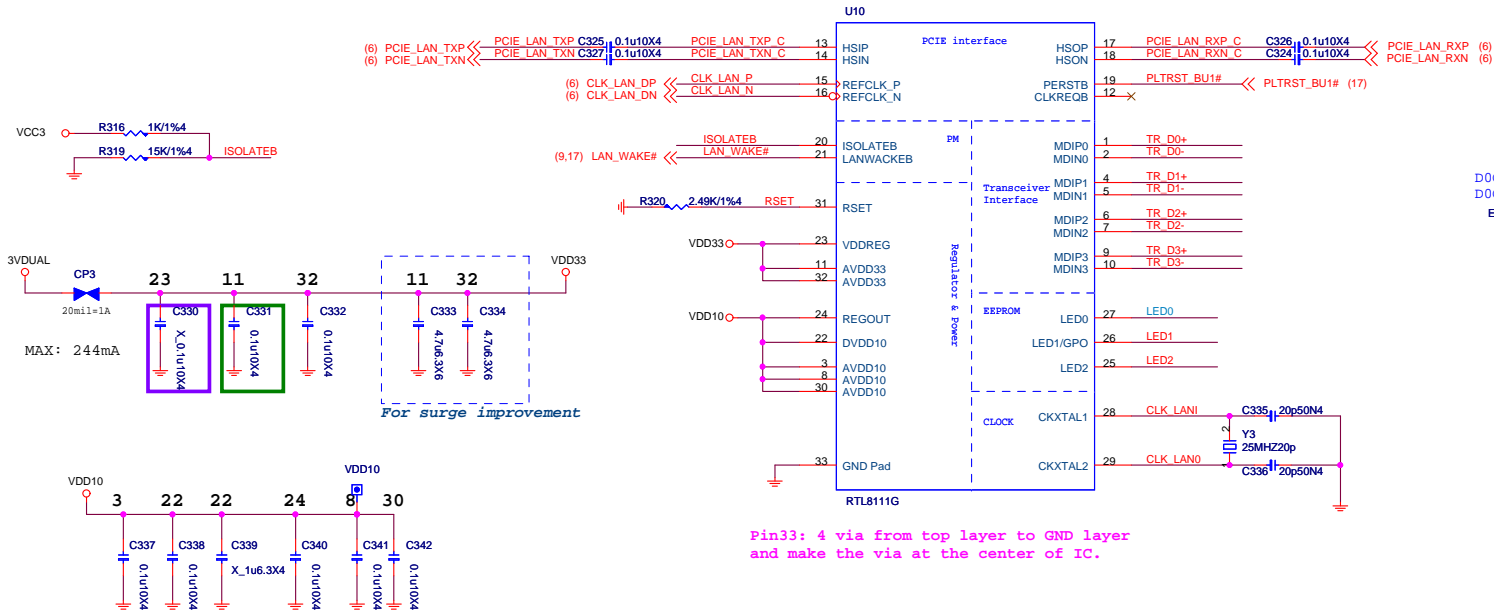
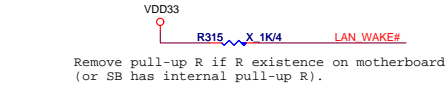


Rear Line OUT De-POP circuit

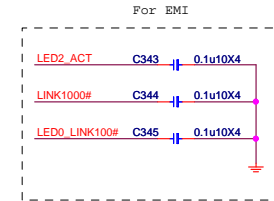
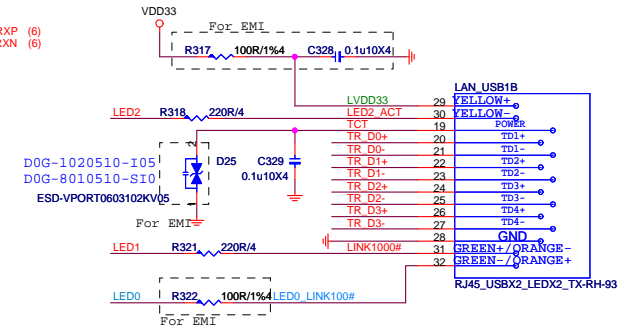
(De-pop circuit for Rear Line out & Front Headphone out)



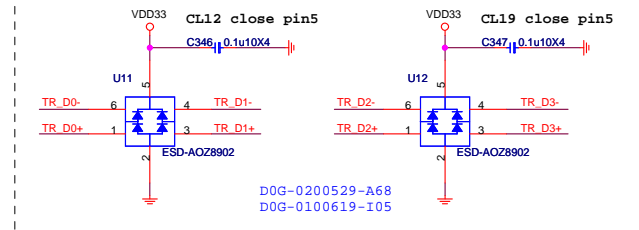
RTL8111G Giga LAN



LAN Connector



ESD Protect

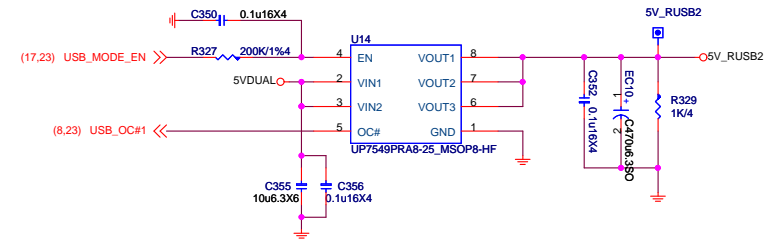
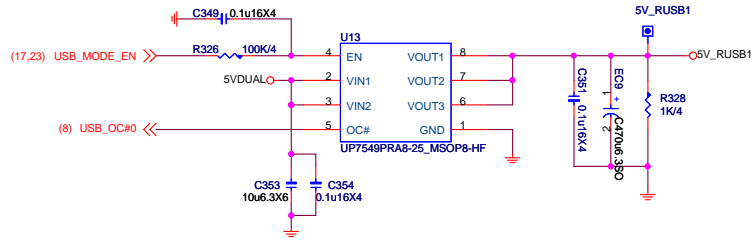


8111G POWER Consumption

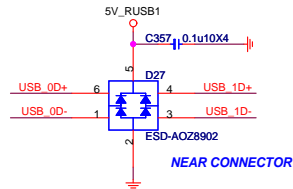
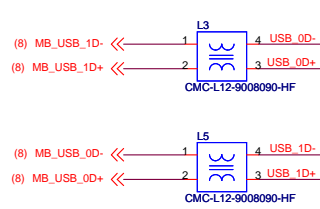
	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

msi MICRO-STAR INT'L CO.,LTD.		
Title MS-G019		
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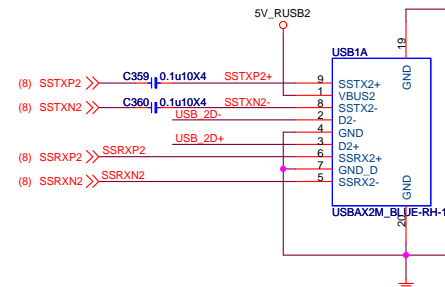
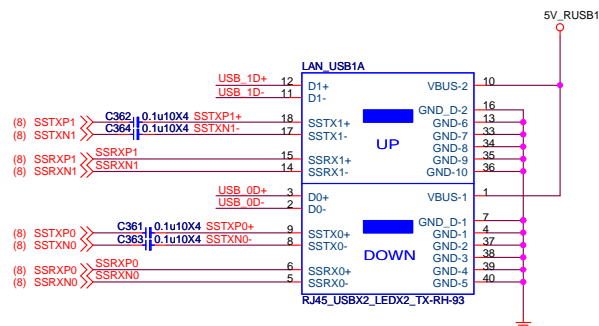
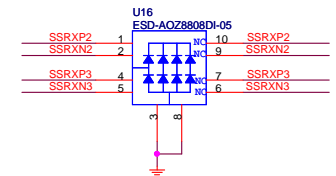
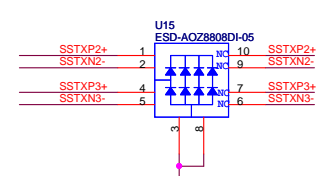
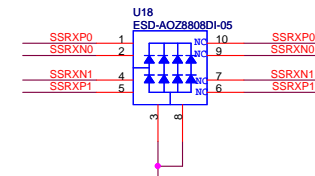
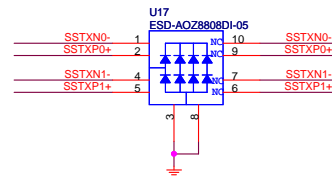
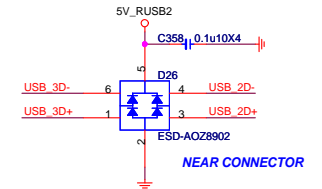
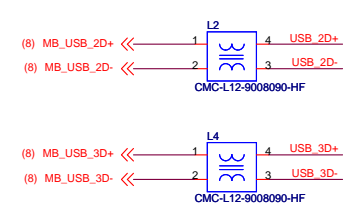
USB POWER: UP7549PRA8-25



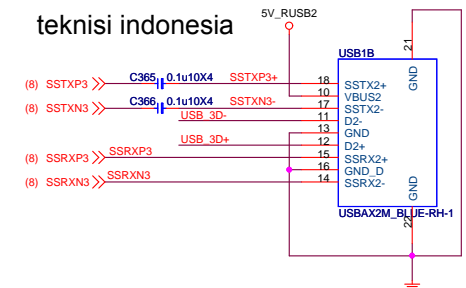
Rear USB PORT 0,1



Rear USB PORT 2,3

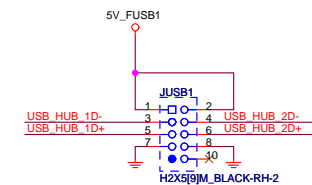
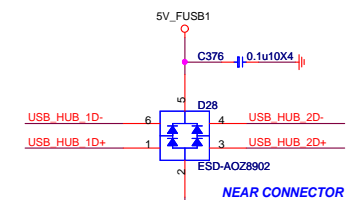
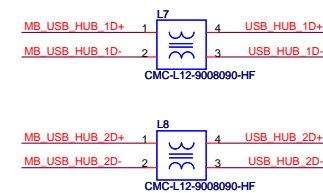
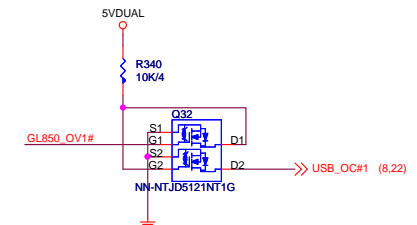
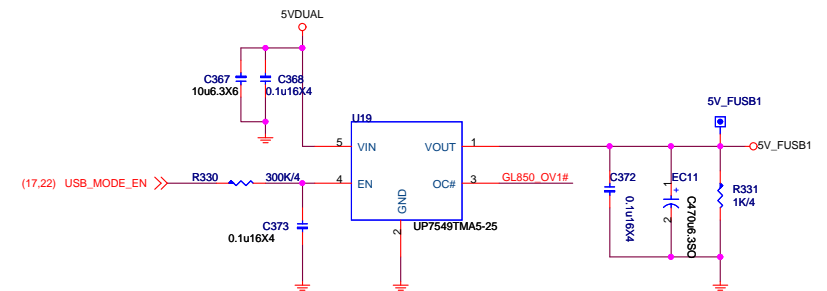
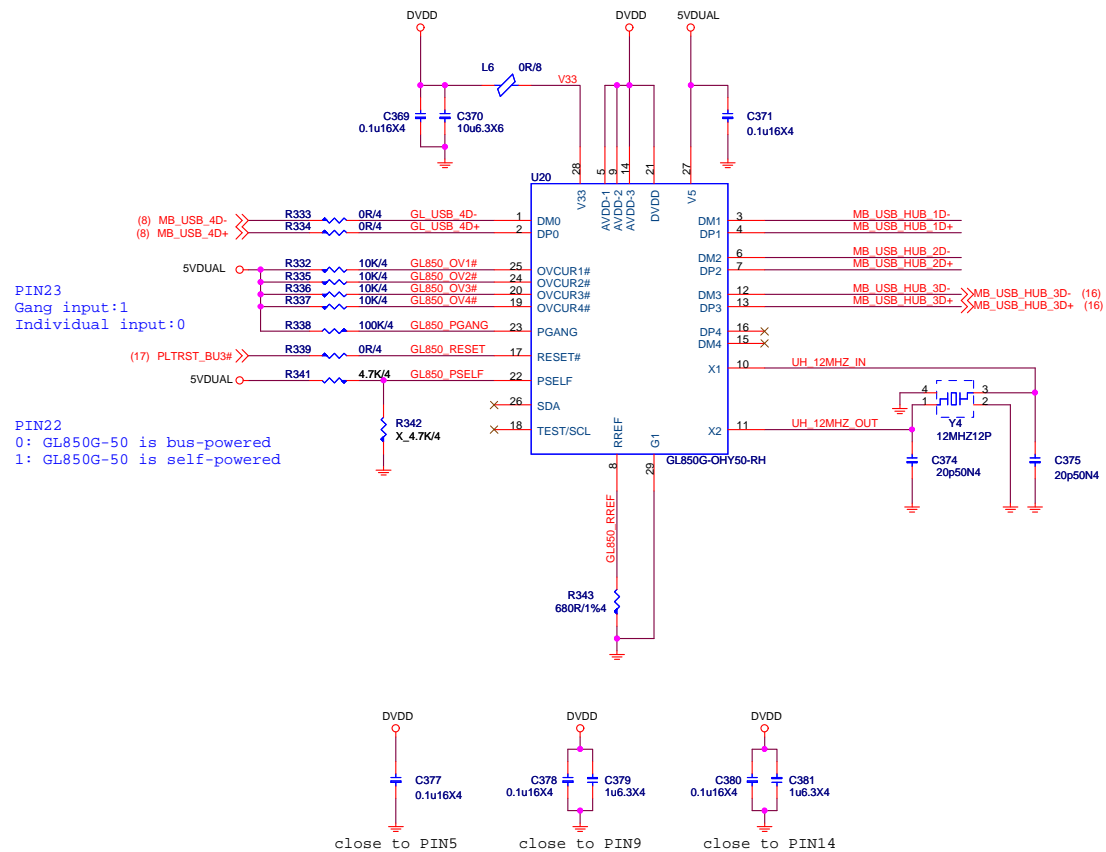


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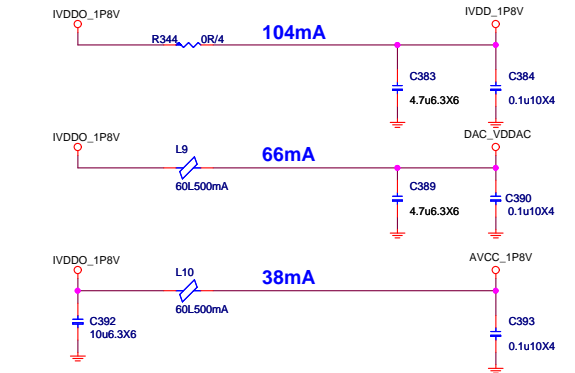
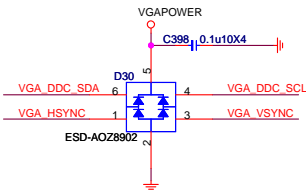
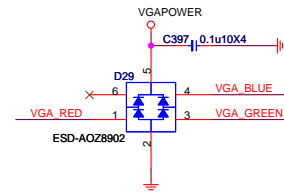
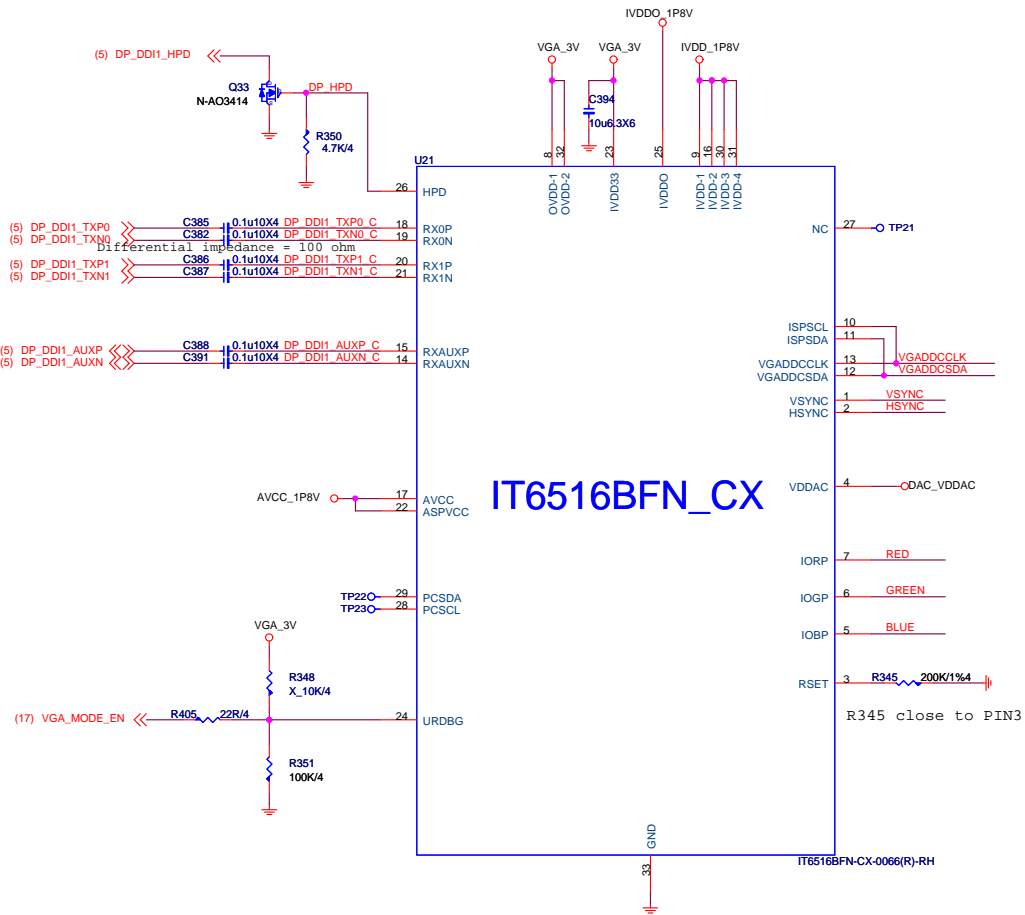


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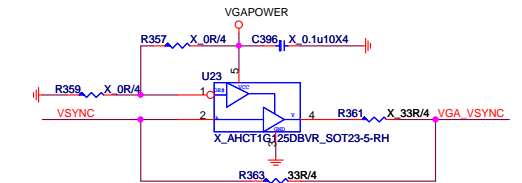
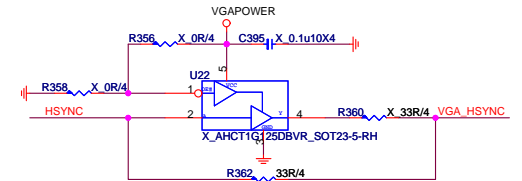
USB HUB



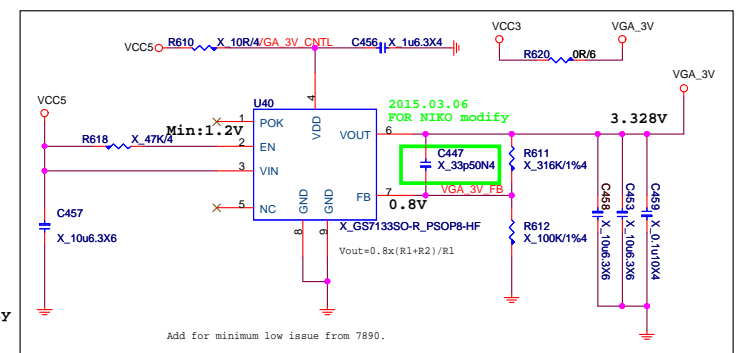
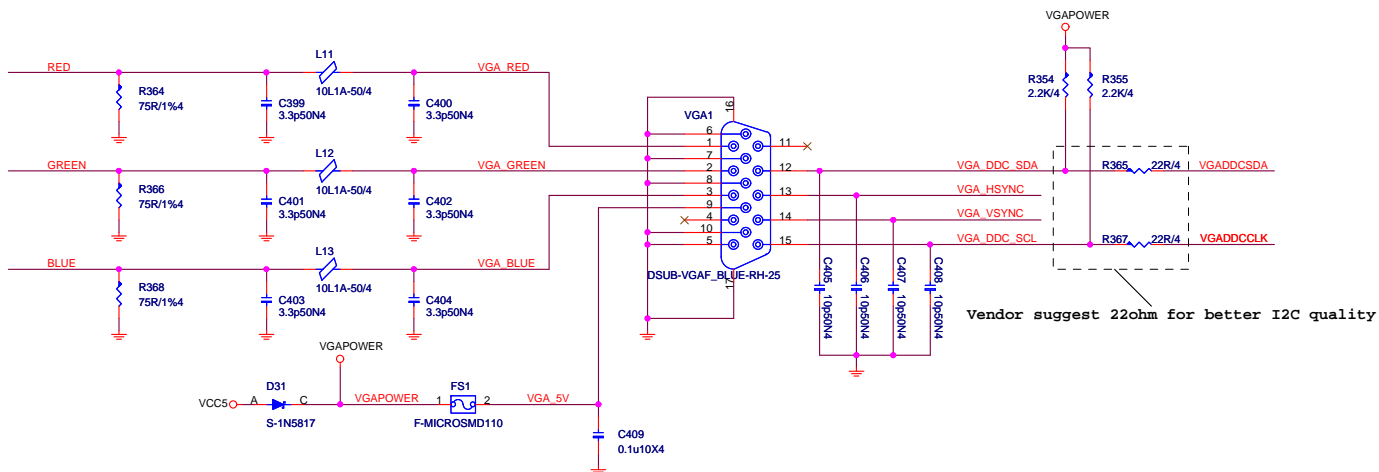
D-Sub



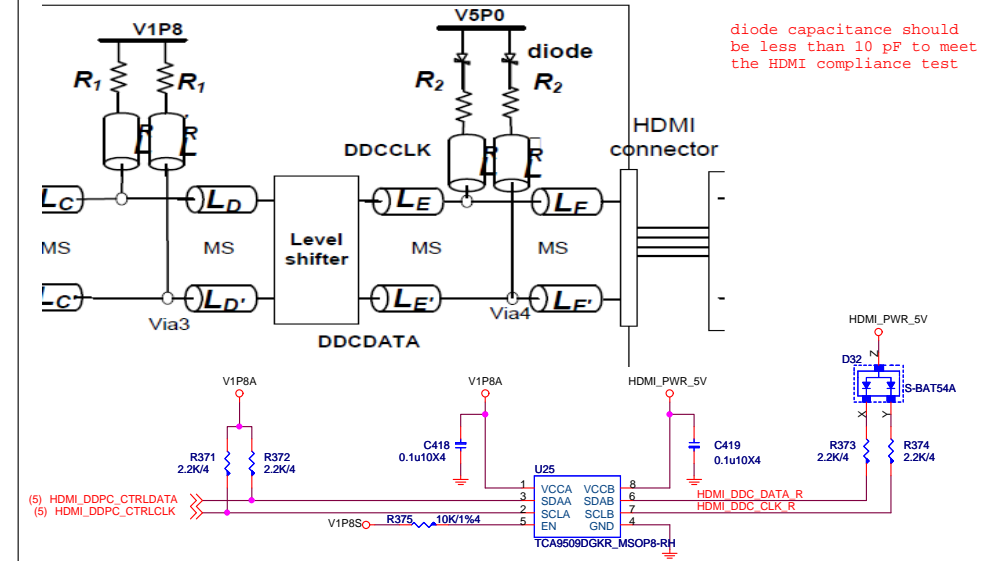
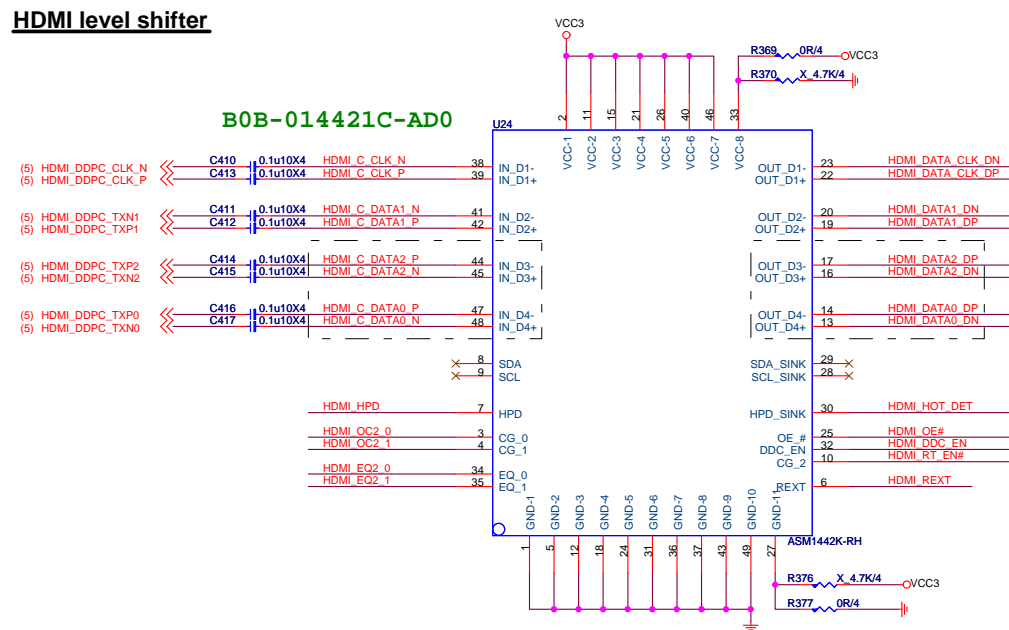
Close to PIN32



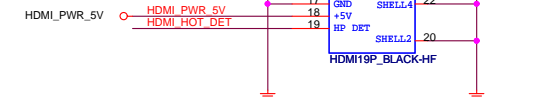
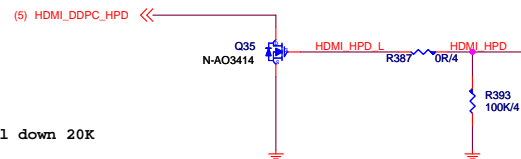
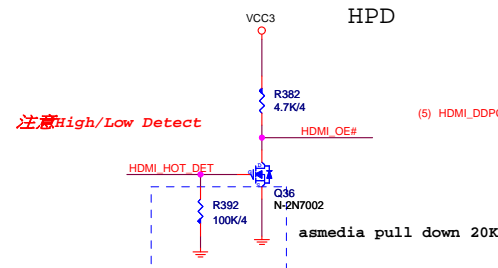
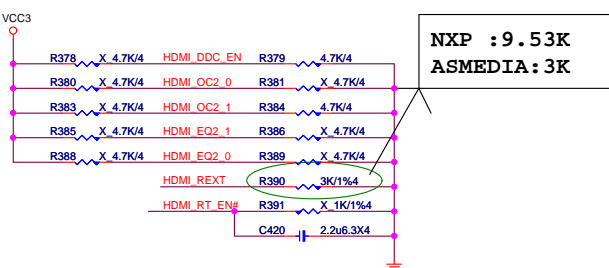
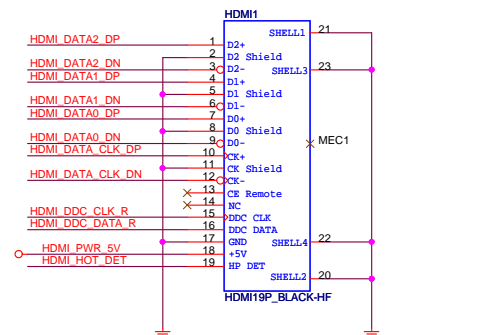
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HDMI level shifter



I9B-9509D12-T07



	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
RESET		

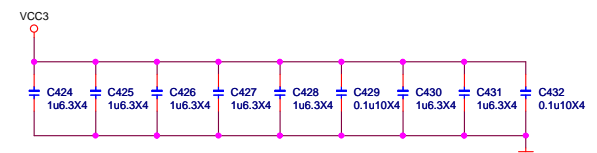
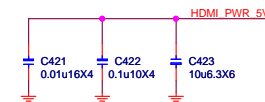
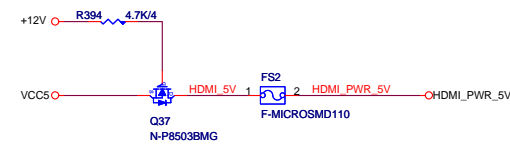
note


- internal pull-up at ~500K ohm.
- internal pull-down at ~500K ohm.
- internal pull-down at ~500K ohm.
- internal pull-down at ~200K ohm; 5V tolerant.
- internal pull-down at ~500K ohm.

analog current generation.

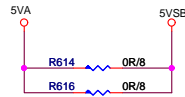
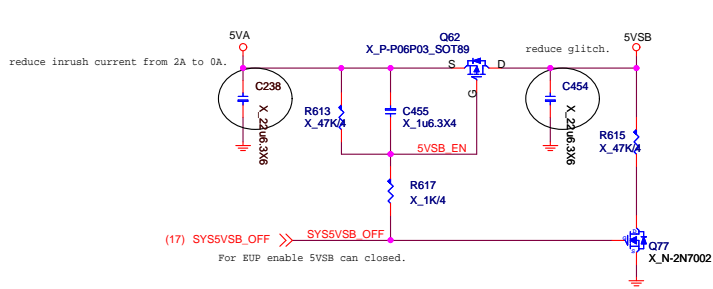
The diagram shows four signal traces over time. Each trace consists of a horizontal red line (low) and a horizontal blue line (high). The transitions are marked with vertical blue lines. The signals are labeled as follows:

- HDMI_DATA_CLK DN** (Red line) and **HDMI_DATA_CLK DP** (Blue line) are connected to **R395 X_100K/1%**.
- HDMI_DATA1 DN** (Red line) and **HDMI_DATA1 DP** (Blue line) are connected to **R396 X_100K/1%**.
- HDMI_DATA2 DN** (Red line) and **HDMI_DATA2 DP** (Blue line) are connected to **R397 X_100K/1%**.
- HDMI_DATA0 DN** (Red line) and **HDMI_DATA0 DP** (Blue line) are connected to **R398 X_100K/1%**.

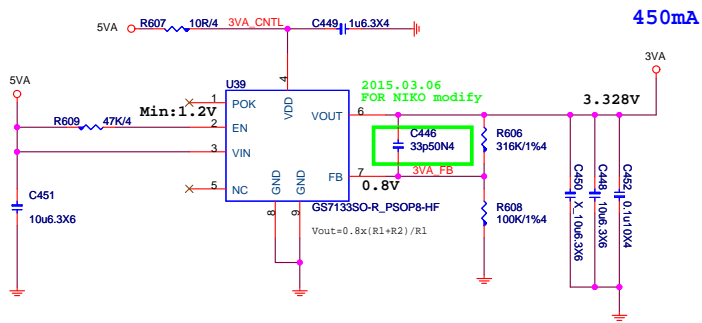


 MICRO-STAR INT'L CO.,LTD.	
Title	
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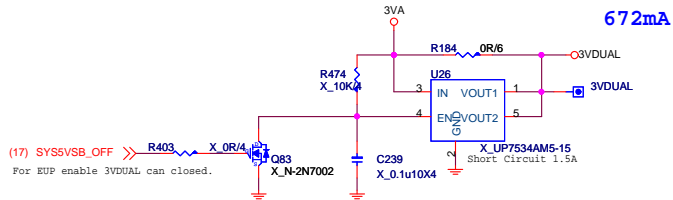
5VSB Power Switch



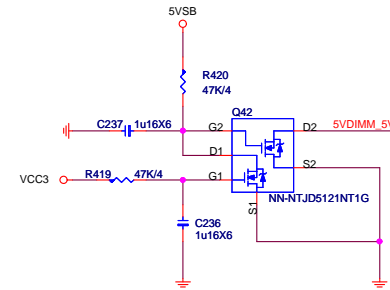
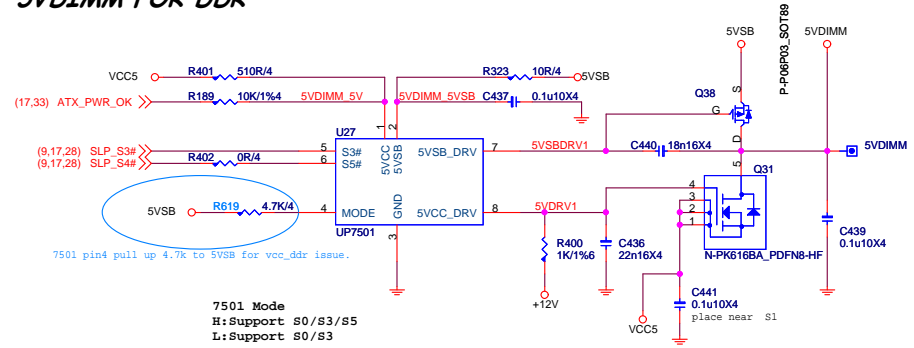
3VA



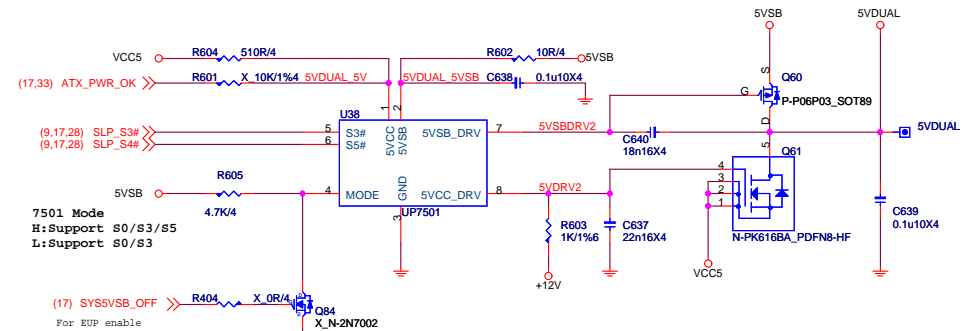
3VDUAL



5VDIMM FOR DDR



5VDUAL

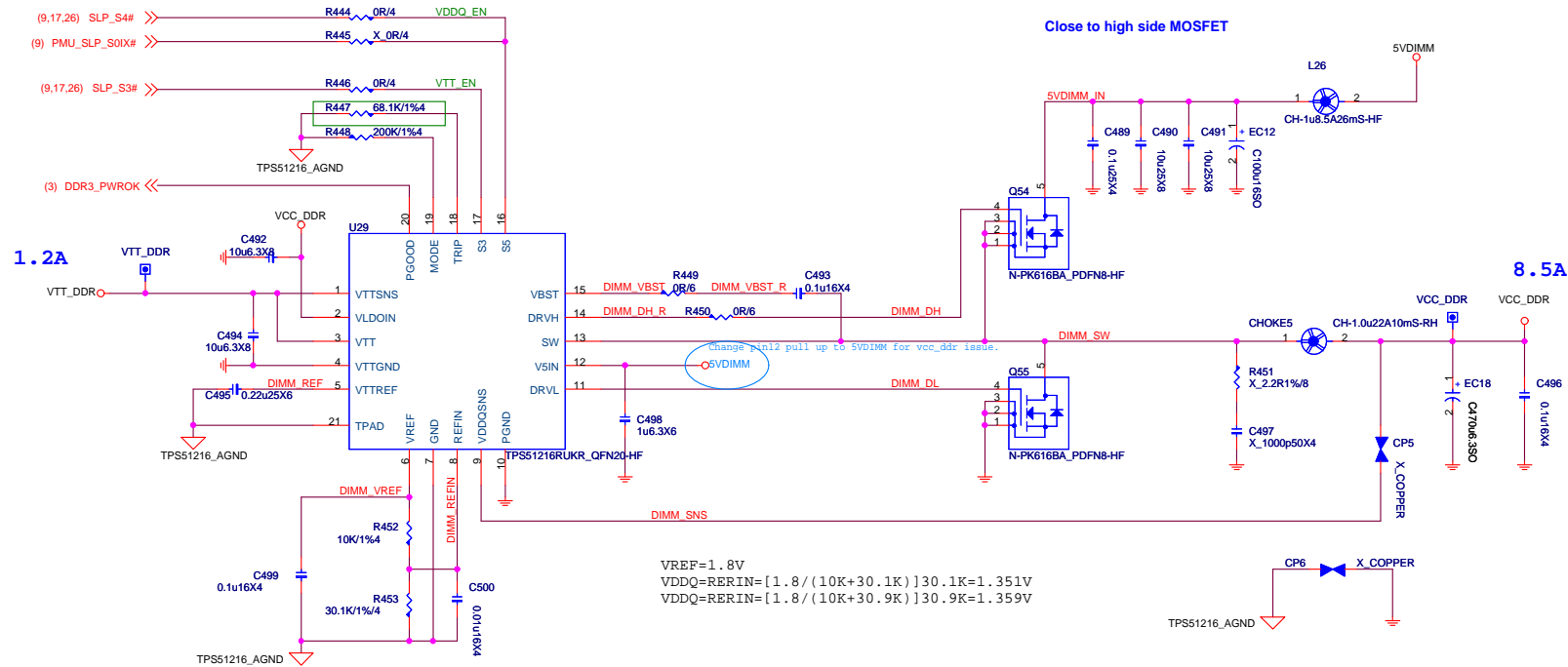


SYSTEM POWER
+5VSUS/+3VSUS/VCC5/VCC3

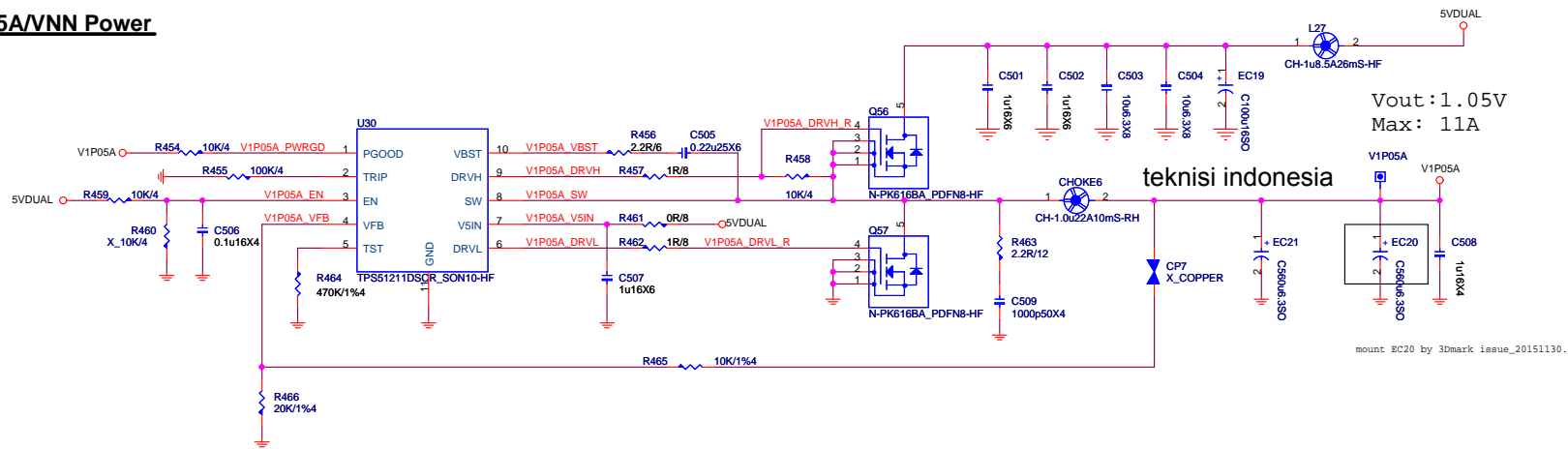
Remove All.

VCC_DDR/VTT_DDR POWER

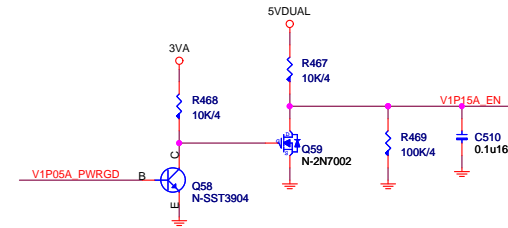
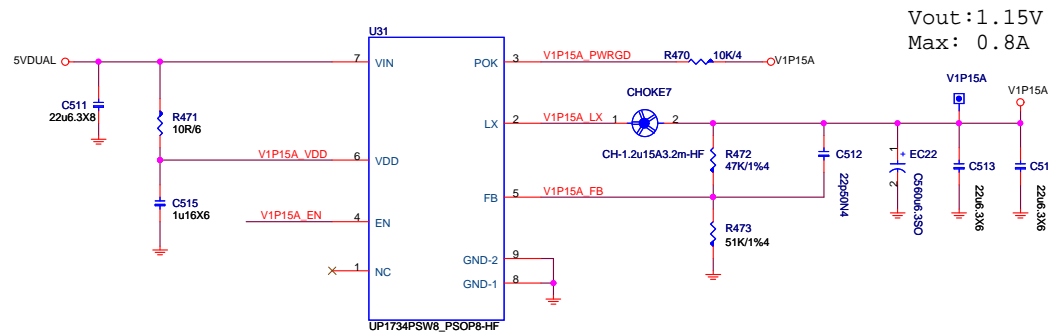
S3/S5 Power State Control						
STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)



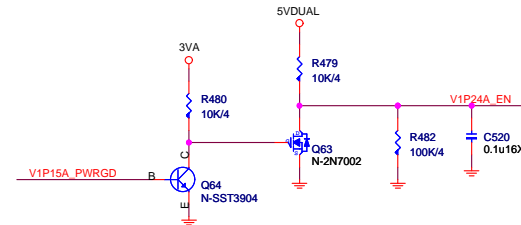
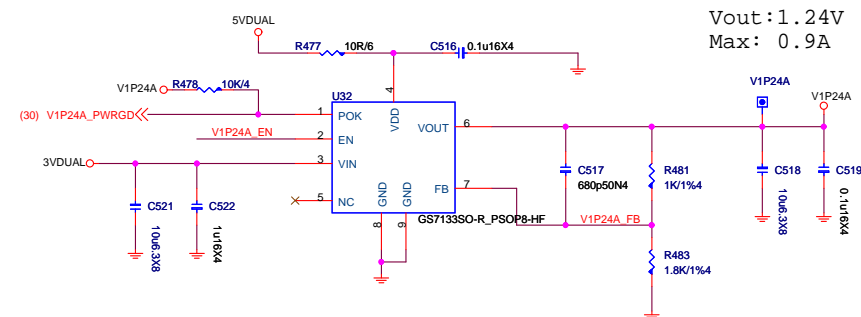
V1P05A/VNN Power



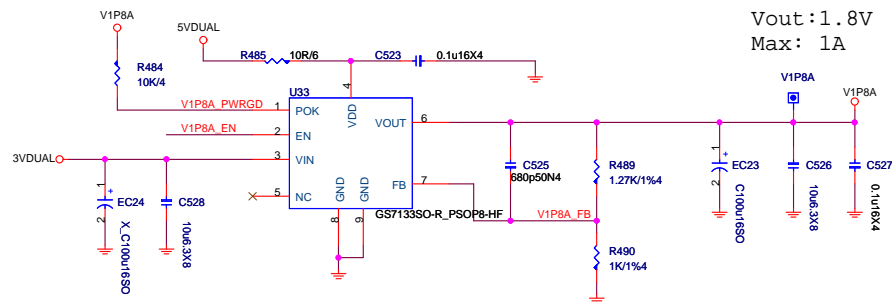
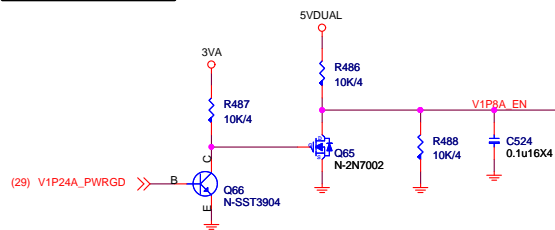
V1P15A Power



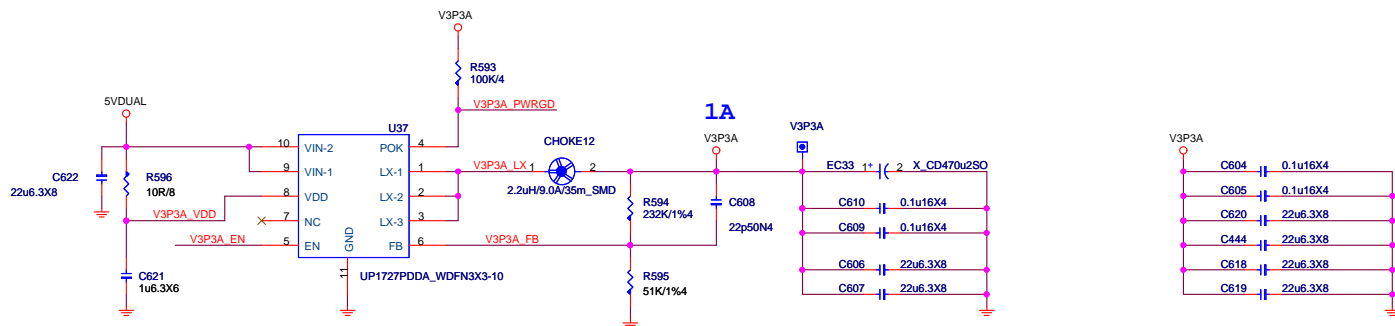
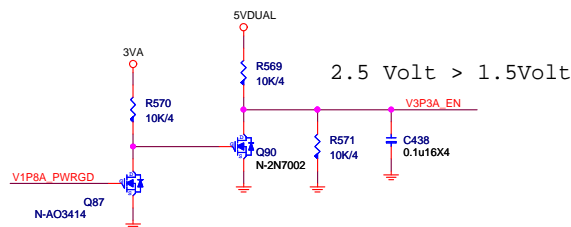
V1P24A POWER



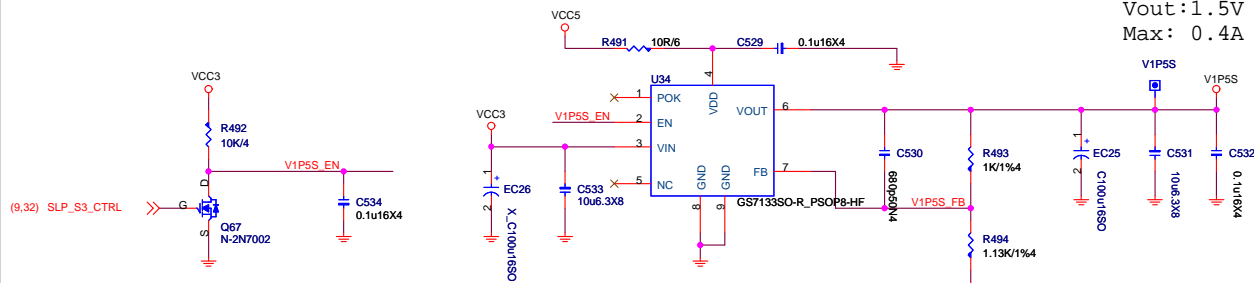
V1P8A POWER



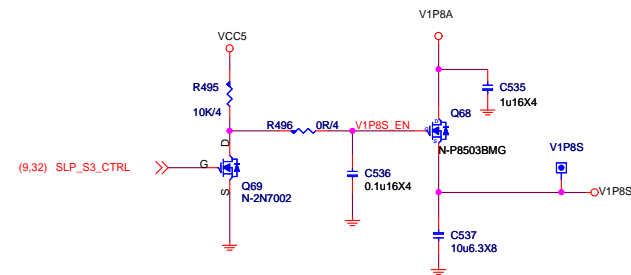
V3P3A POWER



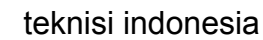
V1P5S Power



V1P8S Power



BRASWELL - VCORE (SVID ADDRESS-00h)



VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
39.2 k	344	391	438	0x4	1.0
48.7 k	438	484	531	0x5	1.0
57.6 k	531	578	625	0x6	1.0
68.1 k	625	676	727	0x7	1.0
78.7 k	727	781	836	0x8	1.1
88.7 k	836	894	953	0x0	1.1
100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1

PUT COLSE
TO VCORE
MOSFET
HOT SPOT

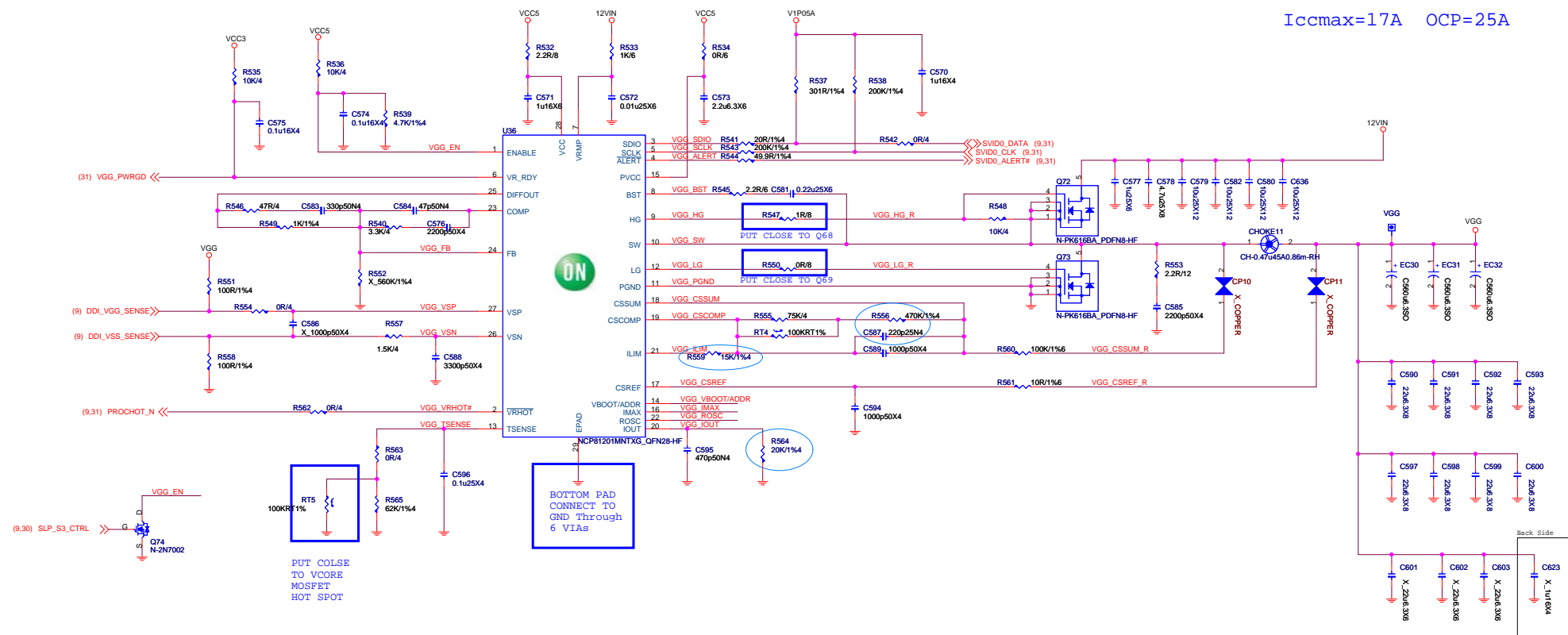
$I_{max} = 10A$

Frequency=400Khz

VGG Power

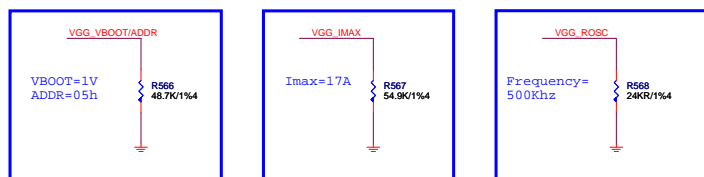
BRASWELL - VGG (SVID ADDRESS-05h)

Iccmax=17A OCP=25A

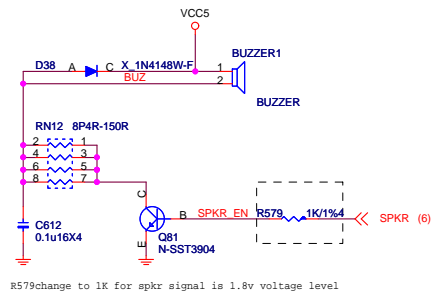


SVID Address and Boot Voltage Table

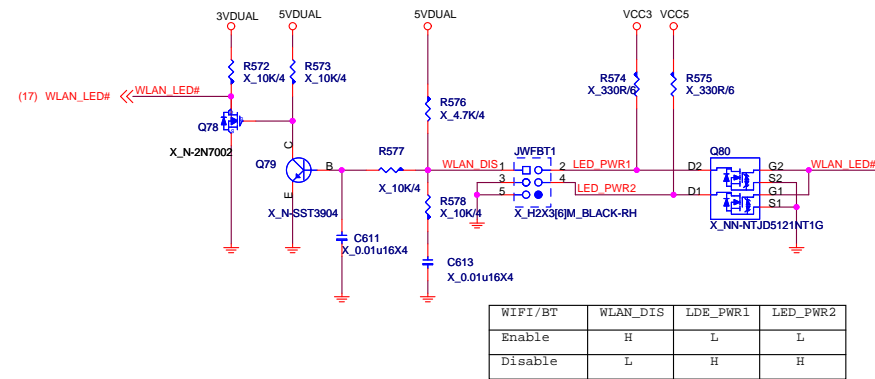
VBOOT/ADDR Resistor (Ohm)	Vboot Pin Voltage (mV)			SVID Address	Vboot (V)
	Min	Typ	Max		
0	0	0	102	0x0	1.0
14.0 k	102	140	180	0x1	1.0
22.1 k	180	219	258	0x2	1.0
30.1 k	258	301	344	0x3	1.0
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78.7 k	727	781	836	0x8	1.1
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100 k	953	1007	1062	0x1	1.1
113 k	1062	1125	1188	0x2	1.1
124 k	1188	1250	1312	0x3	1.1
137 k	1312	1378	1445	0x4	1.1
150 k	1445	1511	1578	0x5	1.1
165 k	1578	1648	1719	0x6	1.1
178 k	1719	1789	1859	0x7	1.1
196 k	1859	1950	-	0x8	1.1



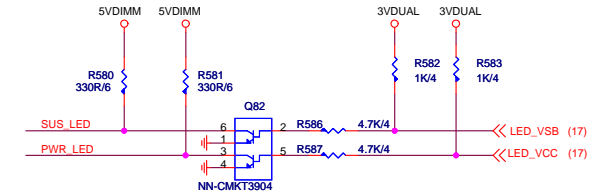
Speaker Pin Header



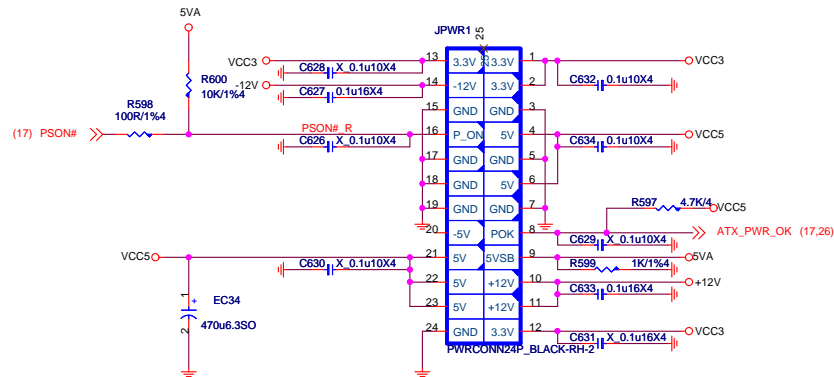
WIFI & BT LED



Power LED

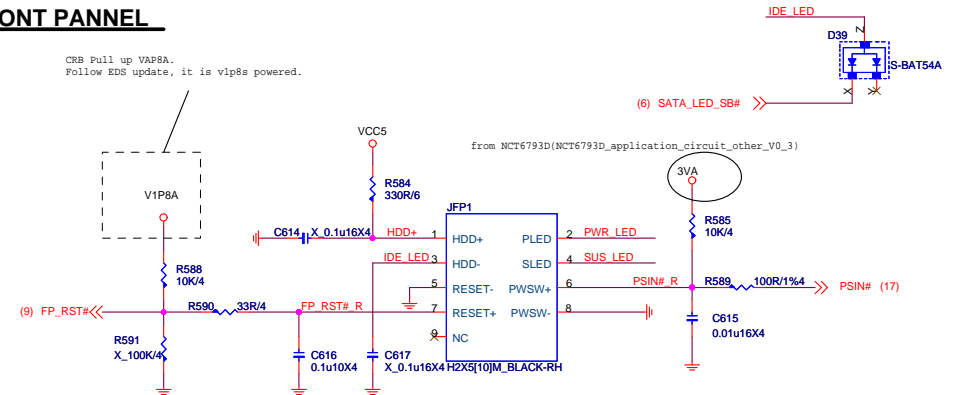


ATX POWER CONNECTOR



FRONT PANNEL

CRB Pull up VAP8A.
Follow EDS update, it is vlp8s powered



EMI

TABLE1
Label
BIOS
BIOS_LABEL

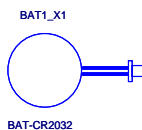
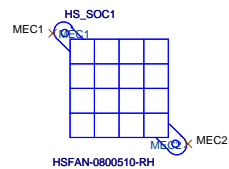
CPU1
CPU
SOC-OPT

TABLE2
Label
HDMI
HDMI_LABEL

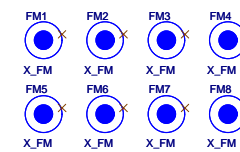
Simulation



SOC



Optical Fiducial Marks-120



Mounting Holes

